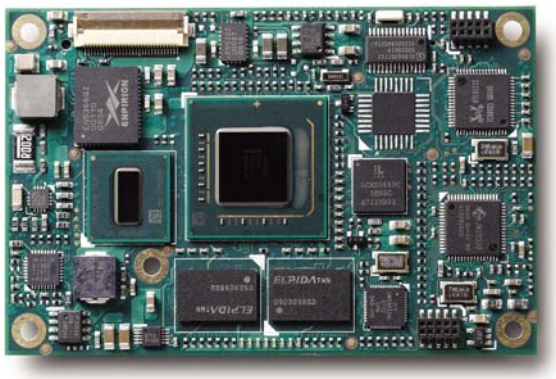
COM Express

Type 1 Compatible

nanoX-ML

User's Manual



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ADLINK TECHNOLOGY INC.

Revision History

Release	Date	Change
2.00	2010/04/22	Initial Release

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

Additional information, aids, and tips that help users perform tasks.

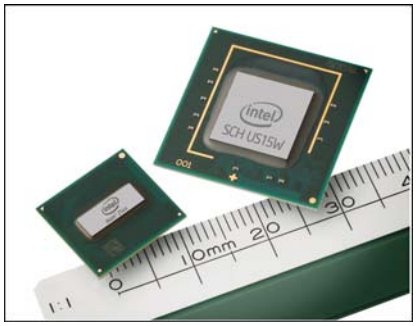
Information to prevent *minor* physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

Information to prevent *serious* physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

1 Introduction

1.1 Description

No bigger in size than a business card, the nanoX-ML is a COM Express™ Type 1 pin compatible computer-on-module that targets battery powered, mobile and handheld system designs. The new Ultra size form factor with a footprint of just 55 mm x 84 mm is the smallest size in ADLINK's COM Express product lineup, next to the Basic size (125 mm x 95 mm) and Compact size (95x95) form factors.



The nanoX-ML is based on the Intel® Atom™ processor Z510 at 1.1 GHz and Z530 at 1.6 GHz processor with a 2 watt thermal design power (TDP). This new 45nm Intel architecture processors implement ground-breaking power management techniques, making them ideal for thermally constrained and fanless embedded applications. Both processors include embedded lifecycle support and remain software compatible with previous 32-bit Intel architectures. The Z530 processor has additional support for Hyper-Threading Technology, a feature introduced with the Intel® Pentium® 4 processor, allowing more than one code thread to be executed simultaneously on a single core processor.

The Intel® System Controller Hub (SCH) US15W, the single chip chipset accompanying the Intel® Atom™ processor, offers an integrated 3D graphics core with dual independent display support on either the integrated 24-bit LVDS or through dual SDVO extension. The true power of the US15Ws graphic core, however, resides in the built-in video hardware decoding that offers acceleration for MPEG2, MPEG4, H.264, WMV9 and VC1. The integrated hardware decoding enables the system to achieve high transfer rates under very modest CPU loading.

The nanoX-ML allows for innovative designs in mobile and "light" computing, including portable and mobile equipment for the automotive and test and measurement industries, visual communication and in the medical field. Using the Intel® Atom™ processor and Intel® SCH US15W chipset, the nanoX-ML allows developers to utilize a wide variety of mainstream software applications and middleware familiar to end users that will run unmodified with full functionality on this platform.

2 Specifications

2.1 General

- Intel® Atom™ Z5xx processor
  - Intel® Atom™ processor Z530 at 1.6 GHz with 533 MHz FSB, 2.2 watts TDP and Hyper-Threading Technology
  - Intel® Atom™ processor Z510 at 1.1 GHz with 400 MHz FSB and 2.0 watts TDP
- Memory: Soldered 256 or 512 MB non-ECC, unbuffered 400/533 MHz DDR2
- Chipset: Intel® System Controller Hub US15W
- L2 Cache: 512 MB
- BIOS: AMIBIOS8 with CMOS backup
- Hardware Monitor: Supply voltages and CPU temperature
- Watchdog Timer: Programmable timer ranges to generate RESET
- Expansion Busses to carrier board:
  - One PCI Express x1 (optional 2nd PCIe x1 lane when LAN is removed)
  - LPC bus
  - SMBus / I^2C

2.2 Video

- Chipset: GMA 500 integrated in System Controller Hub US15W (200 MHz core clock) supports shader-based technology, 2D, 3D and advanced 3D graphics, high-definition video decode, and image processing
- Features: Ultra Low Power Integrated 3D Graphics Core with full HD HW video decode engine and dual independent display support
- CRT Interface: No analog VGA support
- LVDS Interface: Supports single channel 18-bit or 24-bit color and EDID and EDID-less displays with a maximum pixel clock of 112 MHz
- SDVO: May be used for any external display device (HDMI/DVI, analog TV, VGA/CRT and LVDS); includes EDID and EDID-less support, and a 160 MHz pixel clock

2.3 Audio

- Chipset: Integrated in Intel® System Controller Hub US15W
- Type: Intel® High Definition Audio supports up to four audio streams (up to 16 channels each), 32-bit sample depth, sample rates to 192 KHz

2.4 LAN

- Chipset: Realtek RTL8111C PCI Express Gigabit Ethernet Controller
- Interface: 10/100/1000 Mbps with Wake-on-LAN and Alert on LAN support

2.5 Multi I/O

- IDE (PATA): single channel IDE with UDMA (33/66/100) connects to onboard Solid State Drive with 1 GB to 8 GB capacity (Slave)
- SATA: Supports single SATA port via PATA to SATA bridge (Master)
- USB: Eight USB 2.0 ports

2.6 Super I/O

- Connected to LPC bus on carrier if needed (standard support for Winbond W83627HG)

2.7 SDIO/MMC Extension

- Chipset: Integrated in Intel® System Controller Hub US15W
- Type: Single port SDIO/MMC supports SDIO specification 1.1 and MMC specification 4.0
- Connection: Multiplexed over GPIO signals to carrier

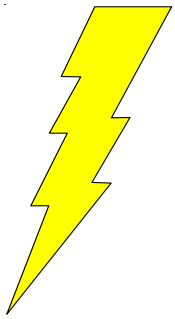
2.8 Operating Systems

- Standard Support
  - Windows Vista
  - Linux 2.6.x
- Extended Support (BSP)
  - Linux BSP
  - AIDI I2C Library for Windows and Linux
  - WinCE 6.0
  - Windows XP Embedded

2.9 Mechanical and Environmental

- Standard Operating Temperature: 0°C to 60°C
- Relative Humidity: up to 90% at 55°C
- Form Factor and Type: PICMG COM.0, COM Express™ Type 1 compatible
- Dimensions: 85 x 44 mm

2.10 Power Specifications



- Input Power: AT mode wide input range 5 V ~ 14 V
  ATX mode wide input range 5 V ~ 14 V and 5 V_{SB}
- Power Management: ACPI 3.0 compliant with smart battery support.

All power testing was done on power supply wiring leading to the Express-BASE carrier board. Although all voltages were measured, only 12 V and 5 V_{SB} are relevant because they are the only ones used by the module.
The *Idle* power level was measured under Windows XP with no applications running (logon screen). *CPU Stress* was measured using Kpower, and *Total System Stress* was measured under burn-in conditions.

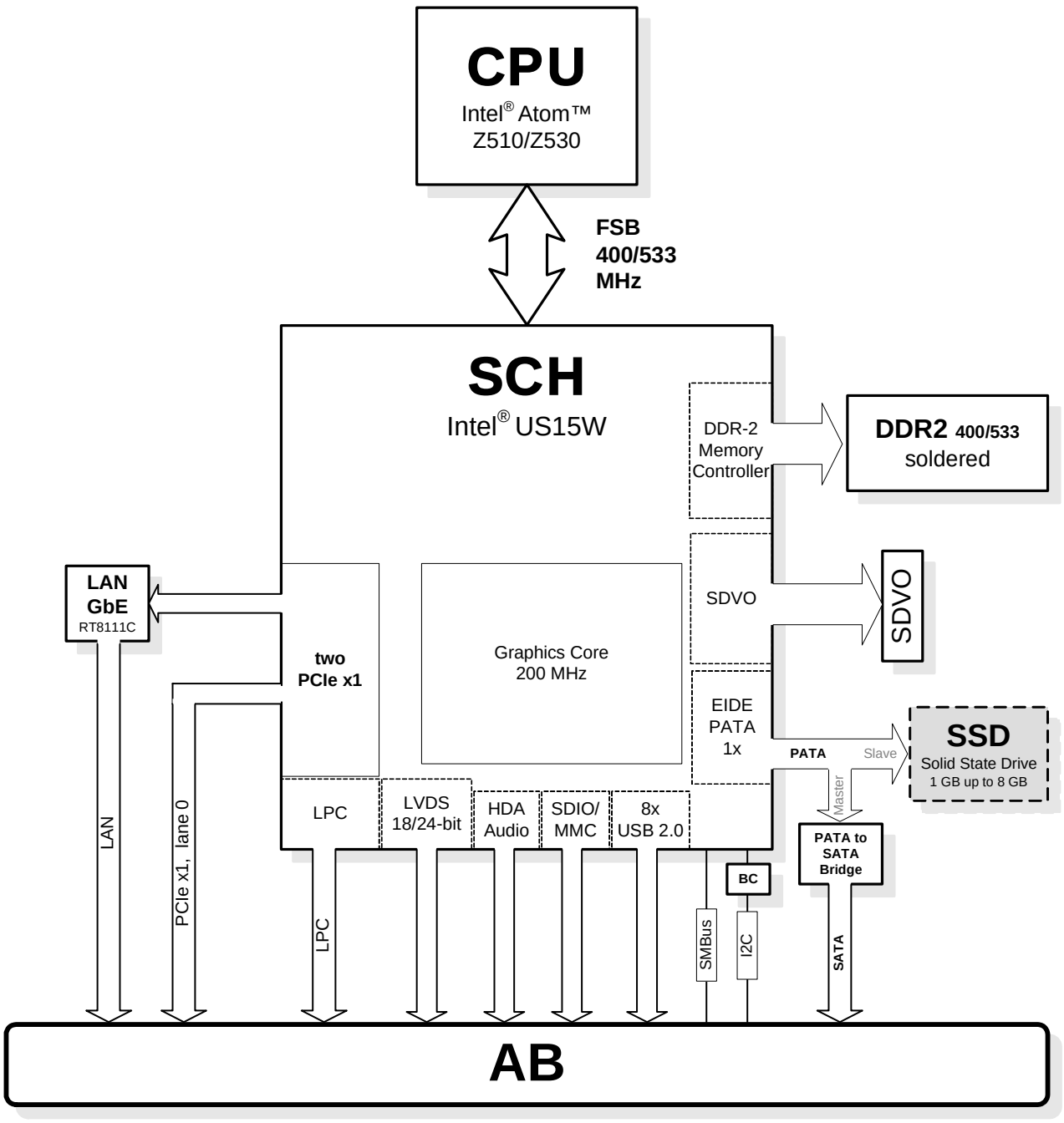
The nanoX-ML was equipped with 512 MB of soldered memory during all tests.

	Power Consumption [A]					Power Consumption [W]			
	12 V	12 V	5 Vsb	5 Vsb		12 V	12 V	5 Vsb	5 Vsb
	Idle WinXP Login	**Max Load** WinXP Burnin/Kpower	**S3** Suspend to RAM	**S5** Soft Off		**Idle** WinXP Login	**Max Load** WinXP Burnin/Kpower	**S3** Suspend to RAM	**S5** Soft Off
nanoX-ML-51	0.35	0.45	0.13	0.11		4.2	5.4	0.7	0.5
nanoX-ML-53	0.34	0.52	0.13	0.11		4.1	6.2	0.7	0.5

2.11 Ordering Codes

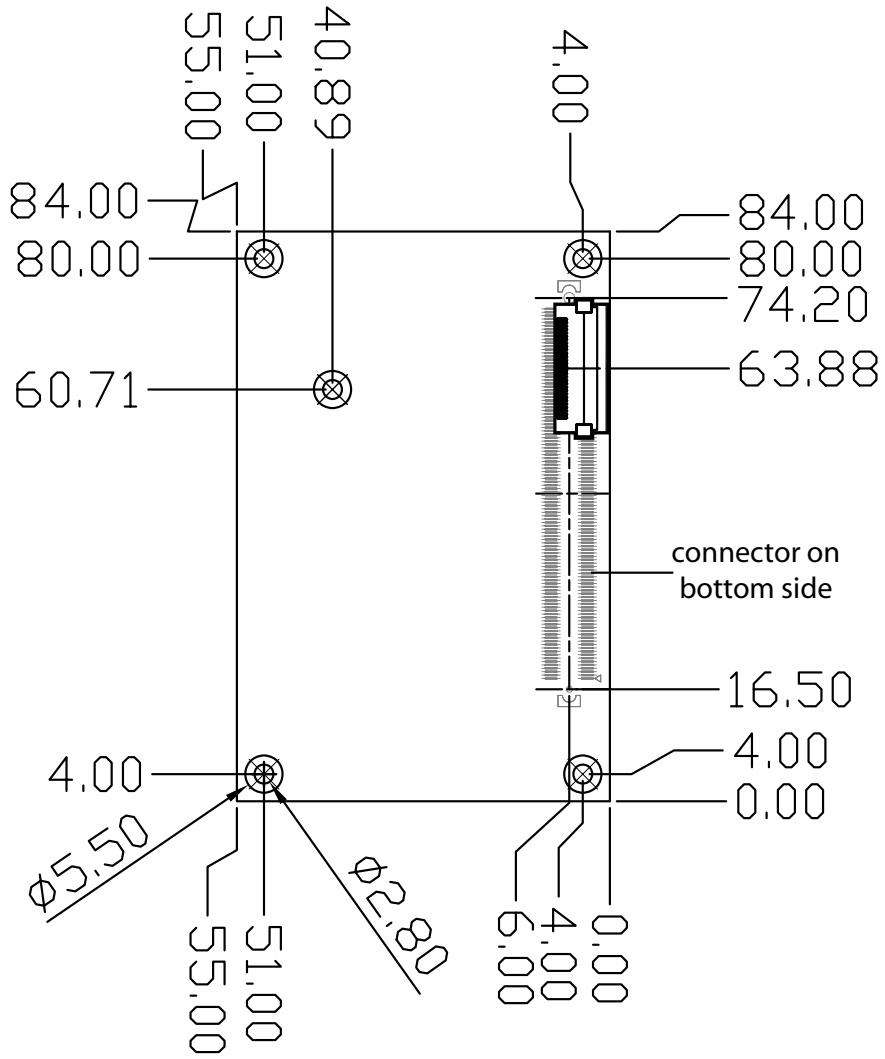
- nanoX-ML-51-512: Ultra size COM Express Type 1 Module with Intel® Atom™ processor Z510 at 1.1 GHz, 512 MB memory
- nanoX-ML-53-512: Ultra size COM Express Type 1 Module with Intel® Atom™ processor Z530 at 1.6 GHz, 512 MB memory
- nanoX-ML-51-512/4G: Ultra size COM Express Type 1 Module with Intel® Atom™ processor Z510 at 1.1 GHz, 512 MB memory and 4 GB SSD storage
- nanoX-ML-53-512/4G: Ultra size COM Express Type 1 Module with Intel® Atom™ processor Z530 at 1.6 GHz, 512 MB memory and 4 GB SSD storage

3 Functional Diagram

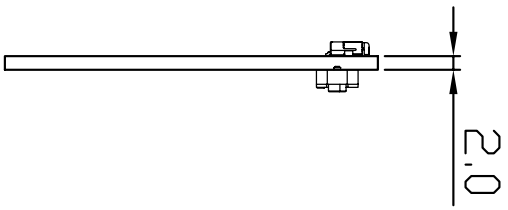


4 Mechanical Dimensions

Top View



Side View



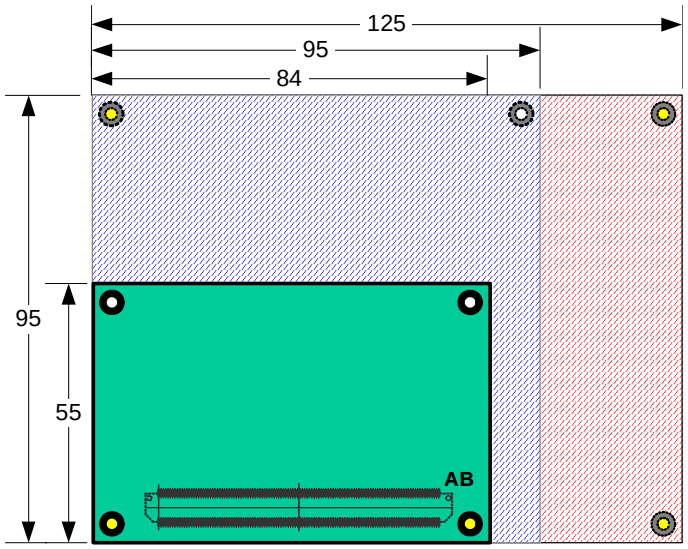
All Ø tolerances ± 0.05 mm
Other tolerances ± 0.2 mm

5 Pinout and Signal Descriptions

5.1 COM Express™ Type 1 Compatible Pinout

All pinouts on AB connector of the nanoX-ML comply with pin-out and signal descriptions used in the “PICMG® COM.0 R1.0: COM Express™ Module Base Specification Type 1”. This chapter details pinouts, signal descriptions, and mechanical characteristics of the nanoX-ML.

An additional document, the “COM Express Design Guide” gives a general introduction to carrier board designs for COM Express™ modules.



- Gigabit Ethernet port
- LPC interface
- 4 Serial ATA channels
- AC'97 or High Definition Audio
- 8 USB 2.0 ports
- 6 PCI Express x1 Lanes
- Dual 24-bit LVDS channels
- Analog VGA
- TV-out ports (SDTV/HDTV)
- GPIO / SDIO
- Keyboard
- I2C / SMBus
- Primary power input: +12V, +5V standby and 3.3V RTC

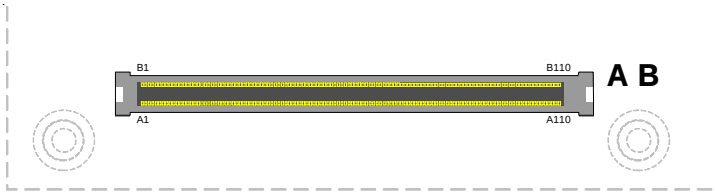
AB Connector

Dimensions in mm

NOTE: The above function mappings are a generic description of COM Express pinouts, and not necessarily supported on the module described in this manual.

5.2 Pin Definitions

Pinouts comply with COM Express Type 1



Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A1	GND (FIXED)		B1	GND (FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#
A3	GBE0_MDI3+		B3	LPC_FRAME#
A4	GBE0_LINK100#		B4	LPC_AD0
A5	GBE0_LINK1000#		B5	LPC_AD1
A6	GBE0_MDI2-		B6	LPC_AD2
A7	GBE0_MDI2+		B7	LPC_AD3
A8	GBE0_LINK#		B8	NC
A9	GBE0_MDI1-		B9	NC
A10	GBE0_MDI1+		B10	LPC_CLK
A11	GND (FIXED)		B11	GND (FIXED)
A12	GBE0_MDI0-		B12	PWRBTN#
A13	GBE0_MDI0+		B13	SMB_CK
A14	NC		B14	SMB_DAT
A15	SUS_S3#		B15	SMB_ALERT#
A16	SATA0_TX+		B16	NC
A17	SATA0_TX-		B17	NC
A18	SUS_S4#		B18	NC
A19	SATA0_RX+		B19	NC
A20	SATA0_RX-		B20	NC
A21	GND (FIXED)		B21	GND (FIXED)
A22	NC		B22	NC
A23	NC		B23	NC
A24	SUS_S5#		B24	PWR_OK
A25	NC		B25	NC
A26	NC		B26	NC
A27	BATLOW#		B27	WDT
A28	ATA_ACT#		B28	AC_SDIN2
A29	AC_SYNC		B29	AC_SDIN1
A30	AC_RST#		B30	AC_SDIN0
A31	GND (FIXED)		B31	GND (FIXED)
A32	AC_BITCLK		B32	SPKR
A33	AC_SDOUT		B33	I2C_CK
A34	BIOS_DISABLE#		B34	I2C_DAT
A35	THRMTRIP#		B35	THRM#
A36	USB6-		B36	USB7-
A37	USB6+		B37	USB7+
A38	USB_6_7_OC#		B38	USB_4_5_OC#
A39	USB4-		B39	USB5-
A40	USB4+		B40	USB5+
A41	GND (FIXED)		B41	GND (FIXED)
A42	USB2-		B42	USB3-
A43	USB2+		B43	USB3+
A44	USB_2_3_OC#		B44	USB_0_1_OC#
A45	USB0-		B45	USB1-
A46	USB0+		B46	USB1+
A47	VCC_RTC		B47	NC
A48	EXCD0_PERST#		B48	NC
A49	EXCD0_CPPE#		B49	SYS_RESET#
A50	LPC_SERIRQ		B50	CB_RESET#
A51	GND (FIXED)		B51	GND (FIXED)
A52	NC		B52	NC
A53	NC		B53	NC
A54	GPI0		B54	GPO1
A55	NC		B55	NC

Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A56	NC		B56	NC
A57	GND		B57	GPO2
A58	NC		B58	NC
A59	NC		B59	NC
A60	GND (FIXED)		B60	GND (FIXED)
A61	NC		B61	NC
A62	NC		B62	NC
A63	GPI1		B63	GPO3
A64	PCIE_TX1+		B64	PCIE_RX1+
A65	PCIE_TX1-		B65	PCIE_RX1-
A66	GND		B66	WAKE0#
A67	GPI2		B67	NC
A68	PCIE_TX0+		B68	PCIE_RX0+
A69	PCIE_TX0-		B69	PCIE_RX0-
A70	GND (FIXED)		B70	GND (FIXED)
A71	LVDS_A0+		B71	NC
A72	LVDS_A0-		B72	NC
A73	LVDS_A1+		B73	NC
A74	LVDS_A1-		B74	NC
A75	LVDS_A2+		B75	NC
A76	LVDS_A2-		B76	NC
A77	LVDS_VDD_EN		B77	NC
A78	LVDS_A3+		B78	NC
A79	LVDS_A3-		B79	LVDS_BKLT_EN
A80	GND (FIXED)		B80	GND (FIXED)
A81	LVDS_A_CK+		B81	NC
A82	LVDS_A_CK-		B82	NC
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT		B84	VCC_5V_SBY
A85	GPI3		B85	VCC_5V_SBY
A86	KBD_RST#		B86	VCC_5V_SBY
A87	KBD_A20GATE		B87	VCC_5V_SBY
A88	PCIE0_CK_REF+		B88	NC
A89	PCIE0_CK_REF-		B89	NC
A90	GND (FIXED)		B90	GND (FIXED)
A91	NC		B91	NC
A92	NC		B92	NC
A93	GPO0		B93	NC
A94	NC		B94	NC
A95	NC		B95	NC
A96	GND		B96	NC
A97	VCC_12V		B97	NC
A98	VCC_12V		B98	NC
A99	VCC_12V		B99	NC
A100	GND (FIXED)		B100	GND (FIXED)
A101	VCC_12V		B101	VCC_12V
A102	VCC_12V		B102	VCC_12V
A103	VCC_12V		B103	VCC_12V
A104	VCC_12V		B104	VCC_12V
A105	VCC_12V		B105	VCC_12V
A106	VCC_12V		B106	VCC_12V
A107	VCC_12V		B107	VCC_12V
A108	VCC_12V		B108	VCC_12V
A109	VCC_12V		B109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)

5.3 Signal Descriptions

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A1	GND	Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A3	GBE0_MDI3+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A4	GBE0_LINK100#	Ethernet Speed LED (100Mb)	OD	-	On at 100Mb/s
A5	GBE0_LINK1000#	Ethernet Speed LED (1000Mb)	OD	-	On at 1000Mb/s
A6	GBE0_MDI2-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A7	GBE0_MDI2+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A8	GBE0_LINK#	LAN Link LED	O-3.3	-	-
A9	GBE0_MDI1-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A10	GBE0_MDI1+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A11	GND	Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A13	GBE0_MDI0+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A14	GBE0_CTREF	ETHCTREF	NC	-	-
A15	SUS_S3#	PM_SLP_S#3	O-3.3	-	-
A16	SATA0_TX+	SATA 0 Transmit Data +	O - DP	-	-
A17	SATA0_TX-	SATA 0 Transmit Data -	O - DP	-	-
A18	SUS_S4#	PM_SLP_S#4	O-3.3	-	-
A19	SATA0_RX+	SATA 0 Receive Data +	I - DP	-	-
A20	SATA0_RX-	SATA 0 Receive Data -	I - DP	-	-
A21	GND	Ground	PWR	-	-
A22	SATA2_TX+	SATA 2 Transmit Data +	NC	-	-
A23	SATA2_TX-	SATA 2 Transmit Data -	NC	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3.3	-	-
A25	SATA2_RX+	SATA 2 Receive Data +	NC	-	-
A26	SATA2_RX-	SATA 2 Receive Data -	NC	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3.3	-	-
A28	ATA_ACT#	ATA_LED# | SATA LED	O-3.3	PU 10k 3.3V	-
A29	AC_SYNC	AC'97 Sync	O-3.3	-	-
A30	AC_RST#	AC'97 Reset	O-3.3	-	-
A31	GND	Ground	PWR	-	-
A32	AC_BITCLK	AC'97 Clock	O-3.3	-	-
A33	AC_SDOUT	AC_SDATAOUT | AC'97 Data	O-3.3	-	-
A34	BIOS_DISABLE#	BIOS_DISABLE#	I-3.3	PU 10k 3.3V	-
A35	THRMTRIP#	PM_THRMTRIP#_CON	O-3.3	PU 1k 3.3V	-
A36	USB6-	USB_PN6 | USB Data - Port6	I/O - DP	-	-
A37	USB6+	USB_PP6 | USB Data + Port6	I/O - DP	-	-
A38	USB_6_7_OC#	USB_OC#_6_7 | USB OverCurrent Port 6/7	I-3.3	PU 10k 3.3Vsb	-
A39	USB4-	USB_PN4 | USB Data - Port4	I/O - DP	-	-
A40	USB4+	USB_PP4 | USB Data + Port4	I/O - DP	-	-
A41	GND	Ground	PWR	-	-
A42	USB2-	USB_PN2 | USB Data - Port2	I/O - DP	-	-
A43	USB2+	USB_PP2 | USB Data + Port2	I/O - DP	-	-
A44	USB_2_3_OC#	USB_OC#_2_3 | USB OverCurrent Port 2/3	I-3.3	PU 10k 3.3Vsb	-
A45	USB0-	USB_PN0 | USB Data - Port0	I/O - DP	-	-
A46	USB0+	USB_PP0 | USB Data + Port0	I/O - DP	-	-
A47	VCC_RTC	V_BAT	PWR	-	-
A48	EXCD0_PERST#	Express Card Support [0] | card reset	O-3.3	-	-
A49	EXCD0_CPPE#	Express Card Support [0] | cap. card req.	I-3.3	-	-
A50	LPC_SERIRQ	INT_SERIRQ | Serial Interrupt Request	IO-3.3	PU 10k 3.3V	-
A51	GND	Ground	PWR	-	-
A52	PCIE5_TX+	PCI Express 5 Transmit +	NC	-	-
A53	PCIE5_TX-	PCI Express 5 Transmit -	NC	-	-
A54	SD0_DATA0	SDIO controller 0 data 0	IO-3.3	-	was GPI0
A55	PCIE4_TX+	PCI Express 4 Transmit +	NC	-	-

Signal Descriptions (cont'd)

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A56	PCIE4_TX-	PCI Express 4 Transmit -	NC	-	-
A57	GND	Ground	PWR	-	-
A58	PCIE3_TX+	PCI Express 3 Transmit +	NC	-	-
A59	PCIE3_TX-	PCI Express 3 Transmit -	NC	-	-
A60	GND	Ground	PWR	-	-
A61	PCIE2_TX+	PCI Express 2 Transmit +	NC	-	-
A62	PCIE2_TX-	PCI Express 2 Transmit -	NC	-	-
A63	SD0_DATA1	SDIO controller 0 data 1	IO-3.3	-	was GPI1
A64	PCIE1_TX+	PCI Express 1 Transmit + (used by LAN)	O - DP	-	remove LAN to use
A65	PCIE1_TX-	PCI Express 1 Transmit - (used by LAN)	O - DP	-	remove LAN to use
A66	GND	Ground	PWR	-	-
A67	SD0_DATA2	SDIO controller 0 data 2	IO-3.3	-	was GPI2
A68	PCIE0_TX+	PCI Express 0 Transmit +	O - DP	-	-
A69	PCIE0_TX-	PCI Express 0 Transmit -	O - DP	-	-
A70	GND	Ground	PWR	-	-
A71	LVDS_A0+	LVDS_AP0 | LVDS Channel A	O - DP	-	-
A72	LVDS_A0-	LVDS_AN0 | LVDS Channel A	O - DP	-	-
A73	LVDS_A1+	LVDS_AP1 | LVDS Channel A	O - DP	-	-
A74	LVDS_A1-	LVDS_AN1 | LVDS Channel A	O - DP	-	-
A75	LVDS_A2+	LVDS_AP2 | LVDS Channel A	O - DP	-	-
A76	LVDS_A2-	LVDS_AN2 | LVDS Channel A	O - DP	-	-
A77	LVDS_VDD_EN	LVDS_VDDEN | LVDS Panel Power	O-2,5	PD 100k	-
A78	LVDS_A3+	LVDS_AP3 | LVDS Channel A	O - DP	-	-
A79	LVDS_A3-	LVDS_AN3 | LVDS Channel A	O - DP	-	-
A80	GND	Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_CLKAP | LVDS Channel A	O - DP	-	-
A82	LVDS_A_CK-	LVDS_CLKAN | LVDS Channel A	O - DP	-	-
A83	LVDS_I2C_CK	LVDS_DDCPCLK | JILI I2C Clock	IO-3.3	PU 10k 3.3Vsb	-
A84	LVDS_I2C_DAT	LVDS_DDCPDATA | JILI I2C Data	IO-3.3	PU 10k 3.3Vsb	-
A85	SD0_DATA3	SDIO controller 0 data 3	IO-3.3	-	was GPI3
A86	KBD_RST#	H_RCIN# | Keyboard Reset	I-3.3	PU 10k 3.3Vsb	-
A87	KBD_A20GATE	H_A20GATE	I-3.3	PU 10k 3.3Vsb	-
A88	PCIE_CK_REF+	CLK_PCIE_REF P	O - DP	-	-
A89	PCIE_CK_REF-	CLK_PCIE_REF N	O - DP	-	-
A90	GND	Ground	PWR	-	-
A91	RSVD		NC	-	-
A92	RSVD		NC	-	-
A93	SD0_CLK	SDIO controller 0 clock	O-3.3	-	was GPO0
A94	RSVD		NC	-	-
A95	RSVD		NC	-	-
A96	GND	Ground	PWR	-	-
A97	VCC_12V	Power 12V	PWR	-	-
A98	VCC_12V	Power 12V	PWR	-	-
A99	VCC_12V	Power 12V	PWR	-	-
A100	GND	Ground	PWR	-	-
A101	VCC_12V	Power 12V	PWR	-	-
A102	VCC_12V	Power 12V	PWR	-	-
A103	VCC_12V	Power 12V	PWR	-	-
A104	VCC_12V	Power 12V	PWR	-	-
A105	VCC_12V	Power 12V	PWR	-	-
A106	VCC_12V	Power 12V	PWR	-	-
A107	VCC_12V	Power 12V	PWR	-	-
A108	VCC_12V	Power 12V	PWR	-	-
A109	VCC_12V	Power 12V	PWR	-	-
A110	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B1	GND	Ground	PWR	-	-
B2	GBE0_ACT#	LAN_ACTLED# | Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC Frame Indicator	O-3.3	-	-
B4	LPC_AD0	LPC Adress & DATA Bus	IO-3.3	-	-
B5	LPC_AD1	LPC Adress & DATA Bus	IO-3.3	-	-
B6	LPC_AD2	LPC Adress & DATA Bus	IO-3.3	-	-
B7	LPC_AD3	LPC Adress & DATA Bus	IO-3.3	-	-
B8	LPC_DRQ0#	SIO_DRQ#0 | LPC Serial DMA Request 0	NC	-	-
B9	LPC_DRQ1#	SIO_DRQ#1 | LPC Serial DMA Request 1	NC	-	-
B10	LPC_CLK	CLK_SIOEXTPCI	O-3.3	-	-
B11	GND	Ground	PWR	-	-
B12	PWRBTN#	Power Button	I-5	-	-
B13	SMB_CK	SMBus Clock	O-3.3	PU 2k2 3.3Vsb	-
B14	SMB_DAT	SMBus Data	IO-3.3	PU 2k2 3.3Vsb	-
B15	SMB_ALERT#	SMB_ALERT#	I-3.3	PU 10k 3.3Vsb	-
B16	SATA1_TX+	SATA 1 Transmit Data +	NC	-	-
B17	SATA1_TX-	SATA 1 Transmit Data -	NC	-	-
B18	SUS_STAT#	PM_SUS_ STAT#	NC	-	-
B19	SATA1_RX+	SATA 1 Receive Data +	NC	-	-
B20	SATA1_RX-	SATA 1 Receive Data -	NC	-	-
B21	GND	Ground	PWR	-	-
B22	SATA3_TX+	SATA 3 Transmit Data +	NC	-	-
B23	SATA3_TX-	SATA 3 Transmit Data -	NC	-	-
B24	PWR_OK	Power OK	I,5	PU 4K7 3.3V	-
B25	SATA3_RX+	SATA 3 Receive Data +	NC	-	-
B26	SATA3_RX-	SATA 3 Receive Data -	NC	-	-
B27	WDT	Watch Dog Timer	O-3.3	PU 10K 3.3Vsb	-
B28	AC_SDIN2	AC_SDATAIN2	NC	-	-
B29	AC_SDIN1	AC_SDATAIN1	I-3.3	-	-
B30	AC_SDIN0	AC_SDATAIN0	I-3.3	-	-
B31	GND	Ground	PWR	-	-
B32	SPKR	AC_SPKR	O-3.3	-	-
B33	I2C_CK	I2CLK	O-3.3	PU 10k 3.3V	-
B34	I2C_DAT	I2DAT	IO-3.3	PU 10k 3.3V	-
B35	THRM#	PM THRM# CON | Over Temperature	I-3.3	-	-
B36	USB7-	USB_PN7 | USB Data - Port7	I/O - DP	-	-
B37	USB7+	USB_PP7 | USB Data + Port7	I/O - DP	-	-
B38	USB_4_5_OC#	USB_OC#_4_5 | USB OverCurrent Port	I-3.3	PU 10k 3.3Vsb	-
B39	USB5-	USB_PN5 | USB Data- Port5	I/O - DP	-	-
B40	USB5+	USB_PP5 | USB Data+ Port5	I/O - DP	-	-
B41	GND	Ground	I-3.3	-	-
B42	USB3-	USB_PN3 | USB Data- Port3	I/O - DP	-	-
B43	USB3+	USB_PP3 | USB Data+ Port3	I/O - DP	-	-
B44	USB_0_1_OC#	USB_OC#_0_1 | USB OverCurrent Port	I-3.3	PU 10k 3.3Vsb	-
B45	USB1-	USB_PN1 | USB Data- Port1	I/O - DP	-	-
B46	USB1+	USB_PP1 | USB Data+ Port1	I/O - DP	-	-
B47	EXCD1_PERST#	Express Card Support [1] |card reset	O-3.3	-	-
B48	EXCD1_CPPE#	Express Card Support [1] | cap. card req.	I-3.3	-	-
B49	SYS_RESET#	ETX_SYS_RESET# | Reset Input	I-3.3	-	-
B50	CB_RESET#	PCI_RST# | PCI Bus Reset	O-3.3	-	-
B51	GND	Ground	PWR	-	-
B52	PCIE5_RX+	PCI Express 5 Receive +	NC	-	-
B53	PCIE5_RX-	PCI Express 5 Receive -	NC	-	-
B54	SD0_CMD	SDIO Controller 0 Command	IO-3.3	PU 41.2k 3.3V	was GPO1
B55	PCIE4_RX+	PCI Express 4 Recieve +	NC	-	-

Signal Descriptions (cont'd)

Row B

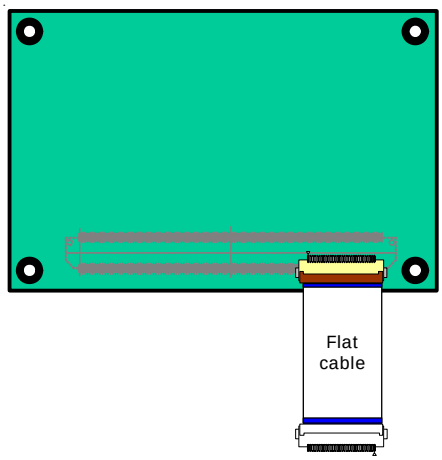
Pin	Signal	Description	Type	PU/PD	Comment
B56	PCIE4_RX-	PCI Express 4 Receive -	NC	-	-
B57	SD0_WP	SDIO Controller 0 Write Protect	IO-3.3	PU 10k 3.3V	was GPO2
B58	PCIE3_RX+	PCI Express 3 Recieve +	NC	-	-
B59	PCIE3_RX-	PCI Express 3 Receive -	NC	-	-
B60	GND	Ground	PWR	-	-
B61	PCIE2_RX+	PCI Express 2 Receive +	NC	-	-
B62	PCIE2_RX-	PCI Express 2 Receive -	NC	-	-
B63	SD0_CD#	SDIO Controller 0 Card Detect	IO-3.3	PU 10k 3.3V	was GPO3
B64	PCIE1_RX+	PCI Express 1 Receive + (used by LAN)	I - DP	-	remove LAN to use
B65	PCIE1_RX-	PCI Express 1 Receive - (used by LAN)	I - DP	-	remove LAN to use
B66	WAKE0#	PCIE_WAKEI#	I-3.3	-	-
B67	WAKE1#	WAKE1#	NC	-	-
B68	PCIE0_RX+	PCI Express 0 Receive +	I - DP	-	-
B69	PCIE0_RX-	PCI Express 0 Receive -	I - DP	-	-
B70	GND	Ground	PWR	-	-
B71	LVDS_B0+	LVDS_BP0 | LVDS Channel B Data0+	NC	-	-
B72	LVDS_B0-	LVDS_BN0 | LVDS Channel B Data0-	NC	-	-
B73	LVDS_B1+	LVDS_BP1 | LVDS Channel B Data1+	NC	-	-
B74	LVDS_B1-	LVDS_BN1 | LVDS Channel B Data1-	NC	-	-
B75	LVDS_B2+	LVDS_BP2 | LVDS Channel B Data2+	NC	-	-
B76	LVDS_B2-	LVDS_BN2 | LVDS Channel B Data2-	NC	-	-
B77	LVDS_B3+	LVDS_BP3 | LVDS Channel B Data3+	NC	-	-
B78	LVDS_B3-	LVDS_BN3 | LVDS Channel B Data3-	NC	-	-
B79	LVDS_BKLT_EN	LVDS Panel Backlight Enable	O-3.3	PD 100k	-
B80	GND	Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_CLKBP | LVDS Channel B	NC	-	-
B82	LVDS_B_CK-	LVDS_CLKBM | LVDS Channel B	NC	-	-
B83	LVDS_BKLT_CTRL	Backlight Brightness	O-3.3	-	-
B84	VCC_5V_SBY	5V Standby	PWR	-	-
B85	VCC_5V_SBY	5V Standby	PWR	-	-
B86	VCC_5V_SBY	5V Standby	PWR	-	-
B87	VCC_5V_SBY	5V Standby	PWR	-	-
B88	RSVD	NC	NC	-	-
B89	VGA_RED	Analog Video RGB-RED	NC	-	-
B90	GND	Ground	PWR	-	-
B91	VGA_GRN	Analog Video RGB-GREEN	NC	-	-
B92	VGA_BLU	Analog Video RGB-BLUE	NC	-	-
B93	VGA_HSYNC	Analog Video H-Sync	NC	-	-
B94	VGA_VSYNC	Analog Video V-Sync	NC	-	-
B95	VGA_I2C_CK	Display Data Channel - Clock	NC	-	-
B96	VGA_I2C_DAT	Display Data Channel - Data	NC	-	-
B97	TV_DAC_A	Composite CVBS	NC	-	-
B98	TV_DAC_B	TV Luminance Signal	NC	-	-
B99	TV_DAC_C	TV Chrominance Signal	NC	-	-
B100	GND	Ground	PWR	-	-
B101	VCC_12V	Power 12V	PWR	-	-
B102	VCC_12V	Power 12V	PWR	-	-
B103	VCC_12V	Power 12V	PWR	-	-
B104	VCC_12V	Power 12V	PWR	-	-
B105	VCC_12V	Power 12V	PWR	-	-
B106	VCC_12V	Power 12V	PWR	-	-
B107	VCC_12V	Power 12V	PWR	-	-
B108	VCC_12V	Power 12V	PWR	-	-
B109	VCC_12V	Power 12V	PWR	-	-
B110	GND	Ground	PWR	-	-

5.4 SDVO Extension

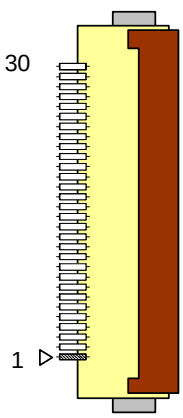
Since COM Express Type 1 only defines the AB connector, the CD connector (COM Express Type 2) which carries the SDVO signals to the carrier is not available. The SDVO signals have been brought out to the carrier using a separate connector.

The SDVO signals are brought out through a Hirose FH12-30S-0.5SH(55), 30-pin FFC/FPC connector located on the top side of the module.

Max routing length from connector to SDVO device is approximately 6", so a cable length of up to 4" can be used.



SDVO Connector Pinout



Pin	Signal	Description	Type
1	GND	Ground	PWR
2	SDVOB_CLK-	SDVO B CLOCK complement	O - DP
3	SDVOB_CLK+	SDVO B CLOCK	O - DP
4	GND	Ground	PWR
5	SDVOB_GREEN-	SDVO B GREEN complement	O - DP
6	SDVOB_GREEN+	SDVO B GREEN	O - DP
7	GND	Ground	PWR
8	SDVOB_INT-	SDVO input interrupt complement.	I - DP
9	SDVOB_INT+	SDVO input interrupt	I - DP
10	GND	Ground	PWR
11	SDVOB_BLU-	SDVO B BLUE complement	O - DP
12	SDVOB_BLU+	SDVO B BLUE	O - DP
13	GND	Ground	PWR
14	SDVOB_RED-	SDVO B RED complement	O - DP
15	SDVOB_RED+	SDVO B RED	O - DP
16	GND	Ground	PWR
17	SDVO_STALL-	SDVO Field Stall complement	I - DP
18	SDVO_STALL+	SDVO Field Stall	I - DP
19	GND	Ground	PWR
20	SDVO_CTRLCLK	I2C control signal (Clock) for SDVO	IO-3.3
21	SDVO_CTRLDAT	I2C control signal (Data) for SDVO	IO-3.3
22	RESET#	RESET signal	O - DP
23	+3.3V	Power supply +3.3V	PWR
24	+2.5V	Power supply +2.5V	PWR
25	+5V	Power supply +5V	PWR
26	GND	Ground	PWR
27	SDVO_TVCLKIN-	SDVO TV-OUT Synchronization Clock complemen	I - DP
28	SDVO_TVCLKIN+	SDVO TV-OUT Synchronization Clock	I - DP
29	+3.3V	Power supply +3.3V	PWR
30	+5V	Power supply +5V	PWR

Signal Description Legend

Signal Type Legend	
IO-2,5	Bi-directional 2,5 V Input/Output
IO-3,3	Bi-directional 3,3 V Input/Output
IO-5	Bi-directional 5 V Input/Output
I-3,3	3,3 V Input
I-5	5 V Input
O-2,5	2,5 V Output
O-3,3	3,3 V Output
O-5	5 V Output
IO	Input/Output
OA	Analog Output
OD	Digital Output
I/O - DP	Differential Pair Input/Output
O - DP	Differential Pair Output
I - DP	Differential Pair Input
PWR	Power or Ground
STO	Strapping Output
PU	Pull Up Resistor
PD	Pull Down Resistor
NC	Not Connected / Reserved

6 Embedded Functions

All embedded board functions on ADLINK's Computer on Modules are supported at the operating system level using the ADLINK Intelligent Device Interface (AIDI) library. The AIDI API programming interface is compatible and identical across all ADLINK Computer on Modules and all supported operating systems. The AIDI library includes a demo program to demonstrate the library's functionallity.

6.1 Watchdog Timer

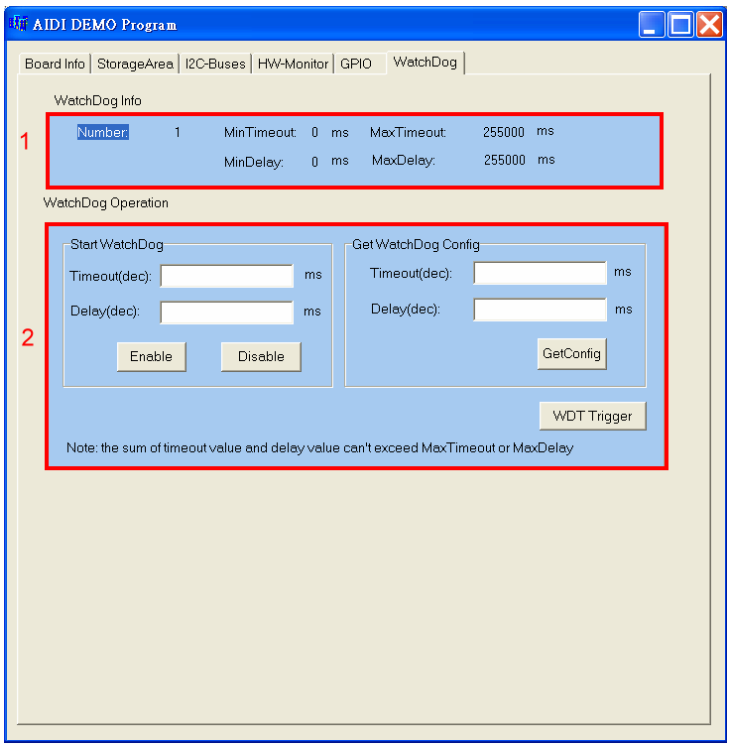
The nanoX-ML implements a watchdog timer that can be used to automatically detect software execution problems or system hangs and reset the board if necessary. The watchdog timer consists of a counter that counts down from an initial value to zero. When the system is operating normally, the software that sets the intial value periodically resets the counter so that the it never reaches zero. If the counter reaches zero before the software resets it, the system is presumed to be malfunctioning and a reset signal is asserted.

The AIDI Library Watchdog Functions support watchdog control of the board. If the watchdog begins countdown and reaches zero, it will access the CPU's RESET signal to reset the system. The watchdog application must call another function named AidiWDogTrigger that restarts the Watchdog timer in order to prevent system reset.

AIDI Demo Program
- Watchdog Tab

The AIDI Demo Program allows retrieval of the current watchdog status and updating of the watchdog settings

If the watchdog is enabled, the user can click the *WDT Trigger* button to manually reset the counter and prevent the system from resetting



6.2 GPIO

GPIO signals can be monitored and controlled by using the ADLINK Intelligent Device Interface (AIDI) library that is compatible and identical across all ADLINK COM Express modules and all supported operating systems.

The nanoX-ML multiplexes GPIO and SDIO signals. On standard modules only SDIO is supported and GPIO is disabled. With a special BOM, SDIO is disabled and GPIO is supported. AIDI support is based on a PCA9535 I2C-to-GPIO device at address 0x40h of the SMBus. For nanoX-ML modules that support SDIO, the PCA9535 device can be placed on the carrier at address 0x40h of the SMBus to obtain transparent support from the AIDI library. Both Express-BASE and nanoX-BASE carrier boards provide the PCA9535 GPIO device.

The COM Express Type 1 standard assigns the following pins for either GPI or GPO

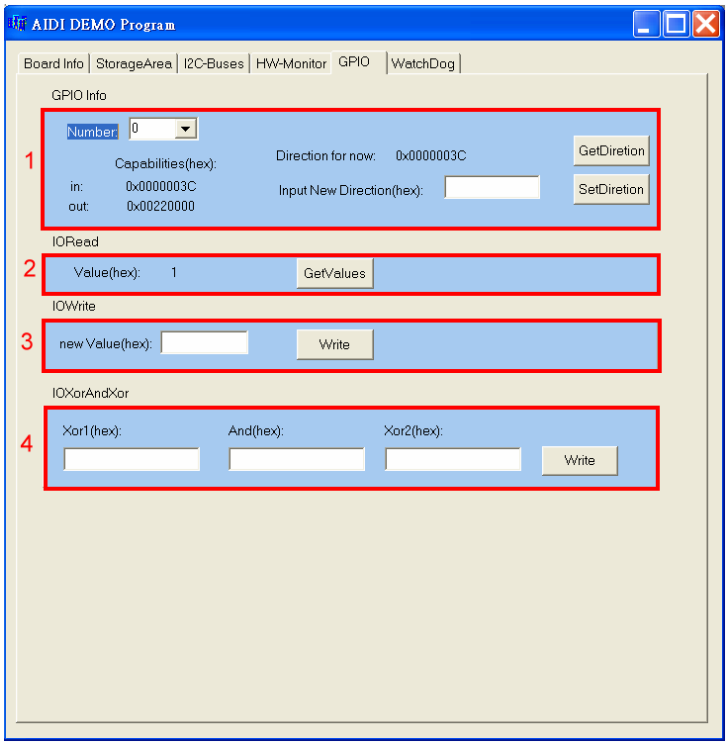
Pin	Signal Type #	AIDI ID (bit)	Remark
A54	GPI0	0	nanoX-ML can configure this pin for GPI and GPO
A63	GPI1	1	nanoX-ML can configure this pin for GPI and GPO
A67	GPI2	2	nanoX-ML can configure this pin for GPI andGPO
A85	GPI3	3	nanoX-ML can configure this pin for GPI andGPO
A93	GPO0	4	nanoX-ML can configure this pin for GPI and GPO
B54	GPO1	5	nanoX-ML can configure this pin for GPI and GPO
B57	GPO2	6	nanoX-ML can configure this pin for GPI and GPO
B63	GPO3	7	nanoX-ML can configure this pin for GPI and GPO

AIDI Demo Program
- GPIO Tab

The AIDI Demo Program displays current GPI or GPO status and allows reading of GPI and writing to GPO.

The table above links logical port numbers in AIDI to physical port numbers on the COM Express board-to-board connector.

For boards that support *multi-direction* the “SetDirection” button can configure the port for either GPI or GPO



6.3 Hardware Monitoring

To ensure system health of your embedded system ADLINK's COM Express modules come with built in support for monitoring and control of CPU and system temperatures, fan speed and critical module voltage levels.

The AIDI Library provides simple APIs at the application level to support these functions and adds alarm functions when voltage or temperature levels exceeds the upper or lower limit set by the user.

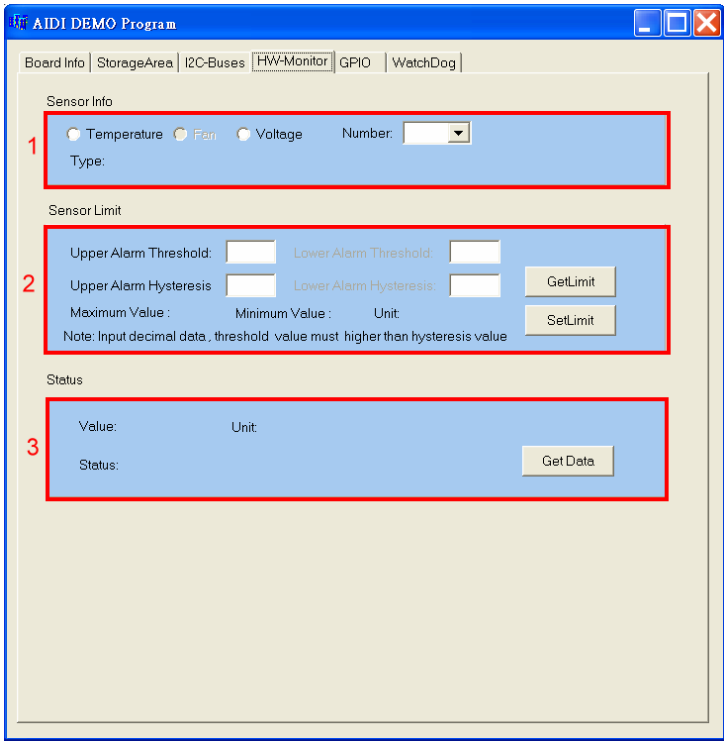
On the nanoX-ML the following monitored values can be read from the module:
CPU temperature, system temperature, Vcore, 1.8 V, 5 V, 3.3 V and 12 V.

AIDI Demo Program
- HW Monitor Tab

Field 1 displays detected sensors (number).

Field 2 allows setting of upper and lower alarm limits.

Field 3 displays read out information of sensors.



7 System Resources

7.1 System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(4 GB - 512 KB)	FFF80000 – FFFFFFFF	512 KB	High BIOS Area
(4 GB - 19 MB) - (4 GB - 18 MB - 1 KB)	FED00000 – FED003FF	1 KB	HPET
(4 GB - 20 MB) - (4 GB - 19 MB - 64 bytes)	FEC00000 – FEC00040	64 bytes	APIC Configuration Space
960 K – 1024 K	F0000 – FFFFF	64 KB	System BIOS Area
896 K – 960 K	E0000 – EFFFF	64 KB	Extended System BIOS Area
768 K – 896 K	C0000 – DFFFF	128 KB	PCI Expansion ROM Area C0000-CEFFF: Onboard VGA BIOS CF000-D0FFF: PXE option ROM when onboard LAN boot ROM is enabled
640 K – 768 K	A0000 – BFFFF	128 KB	Video Buffer & SMM Space
0 K – 640 K	00000 – 9FFFF	640 KB	DOS Area

7.2 Direct Memory Access Channels

Channel Number	Data Width	System Resource	Comment
0	Not Supported (1)		
1	Not Supported (1)		
2	Not Supported (1)		
3	Not Supported (1)		
4	Not Supported (1)		
5	Not Supported (1)		
6	Not Supported (1)		
7	Not Supported (1)		

(1) US15W chipset has no support for DMA.

7.3 Legacy I/O Map

Address (hex)	Size	Description	Comment
0000 – 001F	32 bytes	DMA controller	
0020 – 0021	2 bytes	Interrupt controller	
0024 – 0025	2 bytes	Interrupt controller	
0028 – 0029	2 bytes	Interrupt controller	
002C – 002D	2 bytes	Interrupt controller	
002E - 002F	2 bytes	LPC SIO	
0030 – 0031	2 bytes	Interrupt controller	
0034 – 0035	2 bytes	Interrupt controller	
0038 – 0039	2 bytes	Interrupt controller	
003C – 003D	2 bytes	Interrupt controller	
0040 – 0043	4 bytes	Counter/Timer	
0044 – 0047	4 bytes	System reserved	
0048 – 004B	4 bytes	Counter/Timer	
0050 – 0053	4 bytes	Counter/Timer	
0054 – 005F	12 bytes	System reserved	
0060	1 byte	Keyboard controller	
0061	1 byte	NMI, speaker control	
0063	1 byte	NMI controller	
0064	1 byte	Keyboard controller	
0065	1 byte	NMI controller	
0067	1 byte	NMI controller	
0070 – 0071	2 bytes	Real time clock controller	
0072 – 0073	2 bytes	Real time clock controller	
0074 – 0075	2 bytes	Real time clock controller	
0076 – 0077	2 bytes	Real time clock controller	
0080 – 0091	18 bytes	DMA controller	
0092	1 bytes	Reset Generator	
0093 – 009F	13 bytes	DMA controller	
00A0 – 00A1	2 bytes	Interrupt controller	
00A4 – 00A5	2 bytes	Interrupt controller	
00A8 – 00A9	2 bytes	Interrupt controller	
00AC – 00AD	2 bytes	Interrupt controller	
00B0 – 00B1	2 bytes	Interrupt controller	
00B2 – 00B3	2 bytes	Power Management	
00B4 – 00B5	2 bytes	Interrupt controller	
00B8 – 00B9	2 bytes	Interrupt controller	
00BC – 00BD	2 bytes	Interrupt controller	
00C0 – 00DF	32 bytes	DMA controller	
00E0 – 00EF	16 bytes	System reserved	
00F0 – 00FF	16 bytes	Numeric processor	
01F0 – 01F7	8 bytes	Primary IDE controller	

Legacy I/O Map (cont'd)

Address (hex)	Size	Description	Comment
02F8 – 02FF	8 bytes	COM2	
0378 – 037F	8 bytes	LPT1	
03B0 – 03BB	12 bytes	Video (monochrome)	
03F0 – 03F5, 03F7	7 bytes	Diskette controller	
03F6 – 03F7	2 bytes	Primary IDE controller	
03F8 – 03FF	8 bytes	COM1	
0400 – 041F	32 bytes	Onboard SMBus control registers	
0480 – 04BF	64 bytes	GPIO control registers	
04D0 – 04D1	2 bytes	Edge/level triggered PIC	
0900 – 090F	16bytes	ACPI control registers.	
0900 – 091F	16bytes	Power management registers	
09C0 – 09FF	64bytes	General purpose event block registers	
0CF8 – 0CFF	8 bytes	PCI configuration registers	Note (*)
0CF9	1 byte	Reset control register	Note (**)

(*) DWORD access only
(**) Byte access only

7.4 Interrupt Request (IRQ) Lines

PIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2) / PCI	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1) / PCI	IRQ4 via SERIRQ	Note (1)
5	Parallel Port 2 (LPT2) / PCI	IRQ5 via SERIRQ	Note (1)
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	Parallel Port 1 (LPT1) / PCI	IRQ7 via SERIRQ	Note (1)
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ	Note (1)
10	PCI	IRQ10 via SERIRQ	Note (1)
11	PCI	IRQ11 via SERIRQ	Note (1)
12	PS/2 Mouse / PCI	IRQ12 via SERIRQ	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI	IRQ14 via SERIRQ	Note (1)
15	Secondary IDE controller / PCI	IRQ15 via SERIRQ	Note (1)

NOTE: (1) These IRQs can be used for PCI devices when onboard device is disabled.

APIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2) / PC	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1) / PCI	IRQ4 via SERIRQ	Note (1)
5	Parallel Port 2 (LPT2) / PCI	IRQ5 via SERIRQ	Note (1)
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	Parallel Port 1 (LPT1) / PCI	IRQ7 via SERIRQ	Note (1)
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ	Note (1)
10	PCI	IRQ10 via SERIRQ	Note (1)
11	PCI	SMBus controller	Note (1)
12	PS/2 Mouse / PCI	IRQ12 via SERIRQ	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI	IRQ14 via SERIRQ	Note (1)

APIC Mode (cont'd)

IRQ#	Typical Interrupt Resource	Connected	Available
15	Secondary IDE controller / PCI	IRQ15 via SERIRQ	Note (1)
16	N/A	PCI-E slot, USB, VGA controller, High Definition Audio controller	Yes
17	N/A	USB controller, SD host controller, GbE NIC	Yes
18	N/A	USB controller.	Yes
19	N/A	USB controller	Yes
20	N/A		No
21	N/A		No
22	N/A		No
23	N/A	EHCI, USB	No

(1) These IRQs can be used for PCI devices when onboard device is disabled.

7.5 PCI Configuration Space Map

Bus #	Device #	Function #	Routing	Description	Notes
00h	00h	00h	N/A	Host bridge	
00h	02h	00h	Internal	Intel Integrated Graphics Device	
00h	1Ah	00h	Internal	USB client	
00h	1Bh	00h	Internal	High Definition Audio controller	
00h	1Ch	00h	Internal	PCI Express port 1	
00h	1Ch	01h	Internal	PCI Express port 2	
00h	1Dh	00h	Internal	Intel USB UHCI controller 1	
00h	1Dh	01h	Internal	Intel USB UHCI controller 2	
00h	1Dh	02h	Internal	Intel USB UHCI controller 3	
00h	1Dh	07h	Internal	Intel USB EHCI controller	
00h	1Eh	00h	N/A	SDIO/MMC port 0	
00h	1Eh	01h	N/A	SDIO/MMC port 1	
00h	1Eh	02h	N/A	SDIO/MMC port 2	
00h	1Fh	00h	N/A	Intel LPC interface bridge	
00h	1Fh	01h	Internal	Intel IDE controller	
02h	00h	00h	Onboard	Onboard LAN controller	

8 BIOS Setup Utility

The following chapter describes basic navigation for the AMIBIOS8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:

   < Press DEL or Delete to run Setup >

3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as Chipset and Power menus.

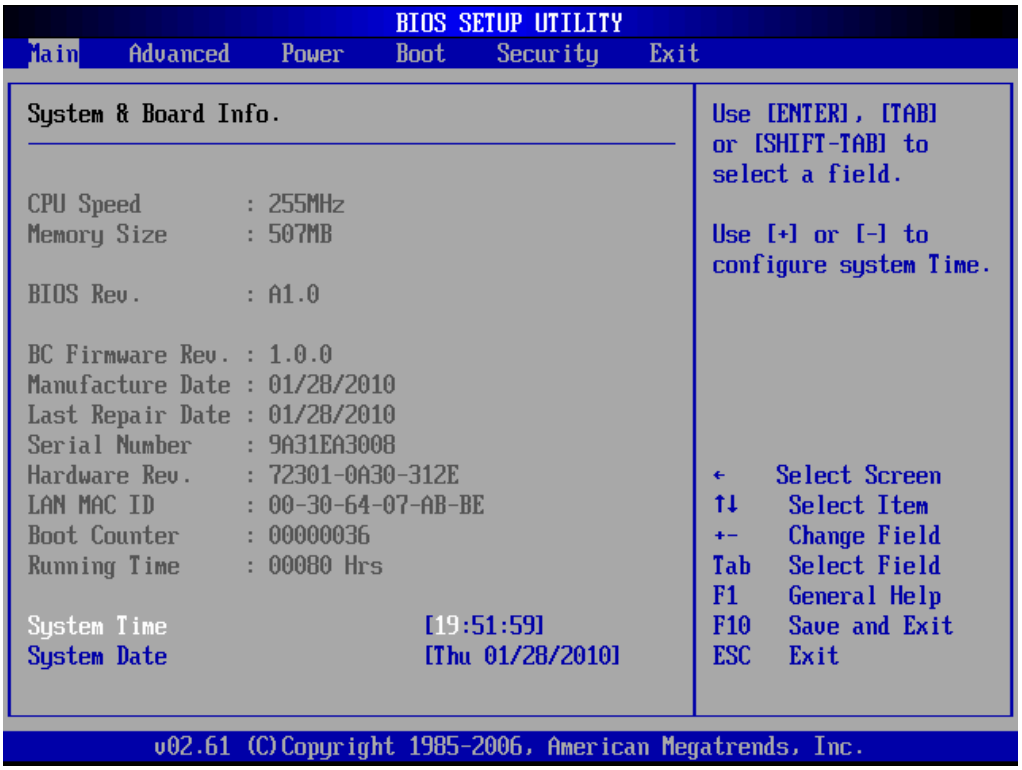
NOTE: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

8.1.1 Main Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

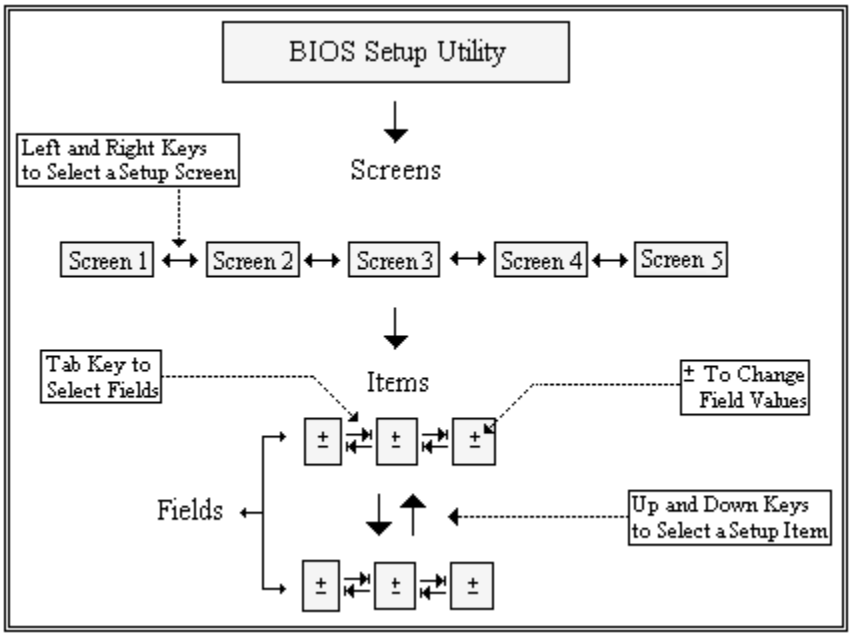
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



8.1.2 Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.
These keys include < F1 >, < F10 >, < Enter >, < ESC >, < Arrow > keys, and so on.

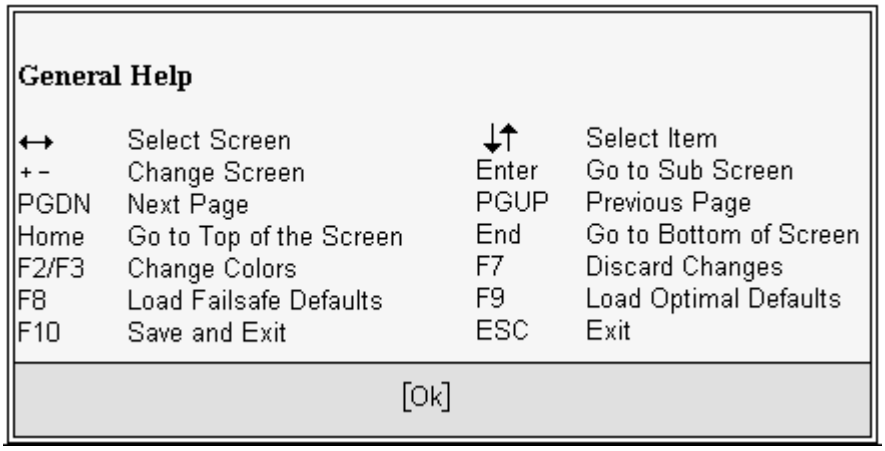


NOTE: There is a hot key legend located in the right frame on most setup screens.

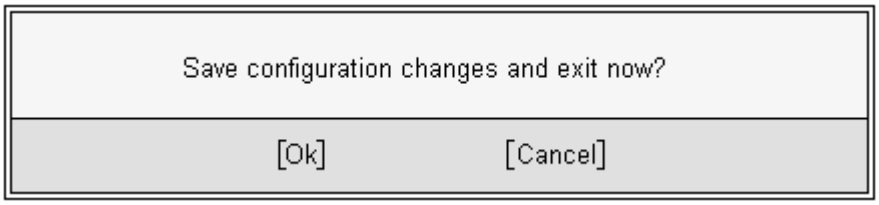
Hot Key	Description
→←	Left/Right The *Left and Right* < Arrow > keys allow you to select a setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓	Up/Down The *Up and Down* < Arrow > keys allow you to select a setup item or sub-screen.
+−	Plus/Minus The *Plus and Minus* < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The < Tab > key allows you to select setup fields.

NOTE: The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

Hot Key	Description
F1	The < F1 > key allows you to display the *General Help screen*. Press the < F1 > key to open the *General Help screen*.

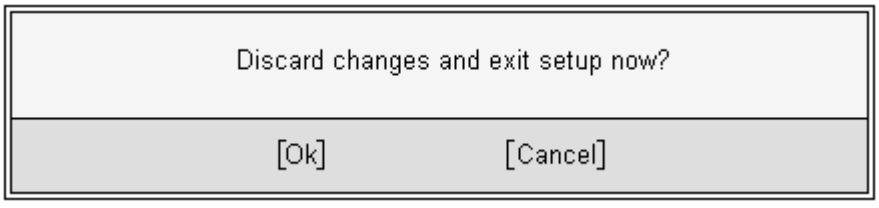


F10	The < F10 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.

ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:

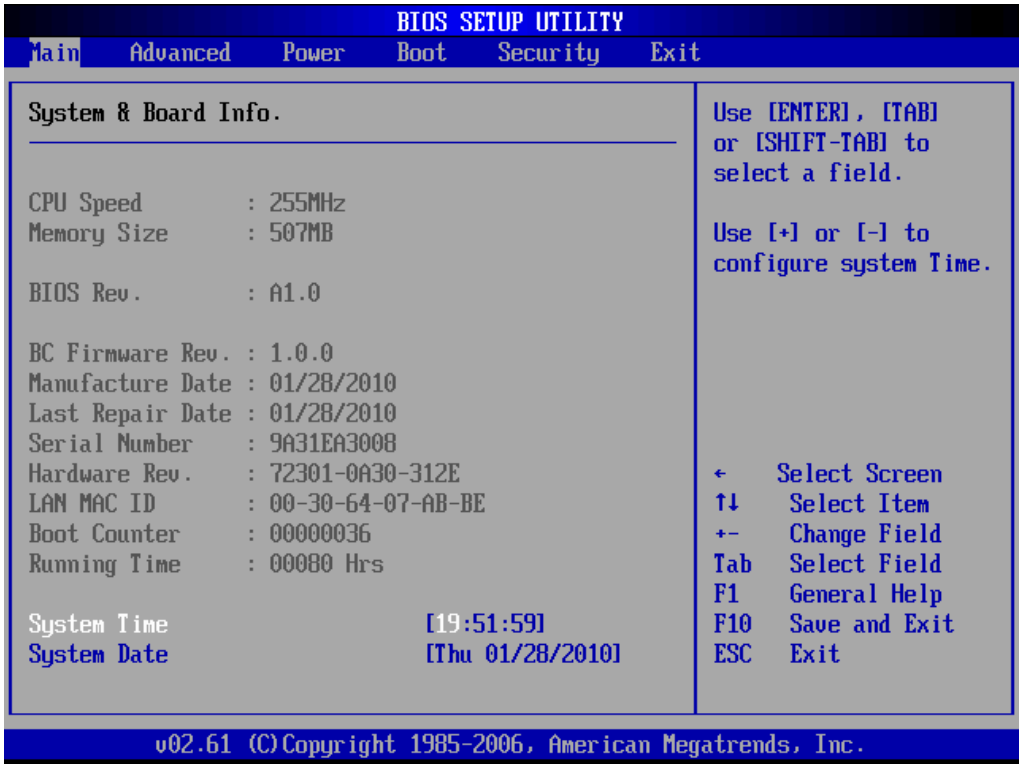


Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.

Enter	The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the *Main* tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



8.2.1 System Time/System Date

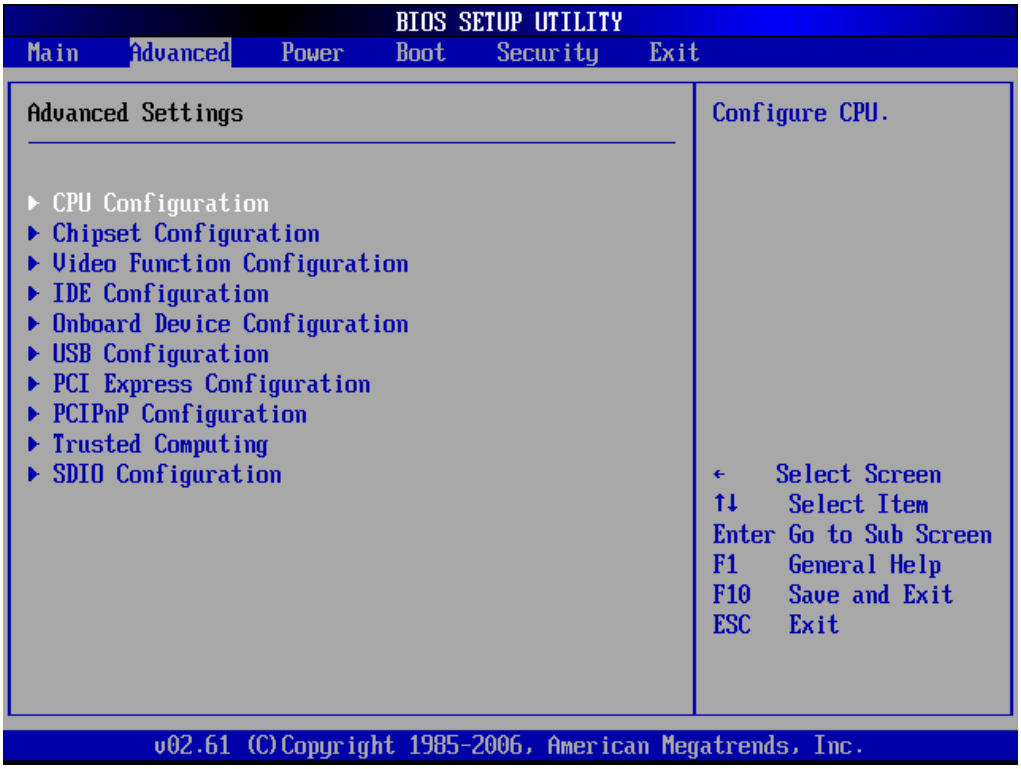
Use this option to change the system time and date. Highlight *System Time* or *System Date* using the < `Arrow` > keys. Enter new values using the keyboard. Press the < `Tab` > key or the
< `Arrow` > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

NOTE: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

8.3 Advanced BIOS Setup

Select the *Advanced* tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.

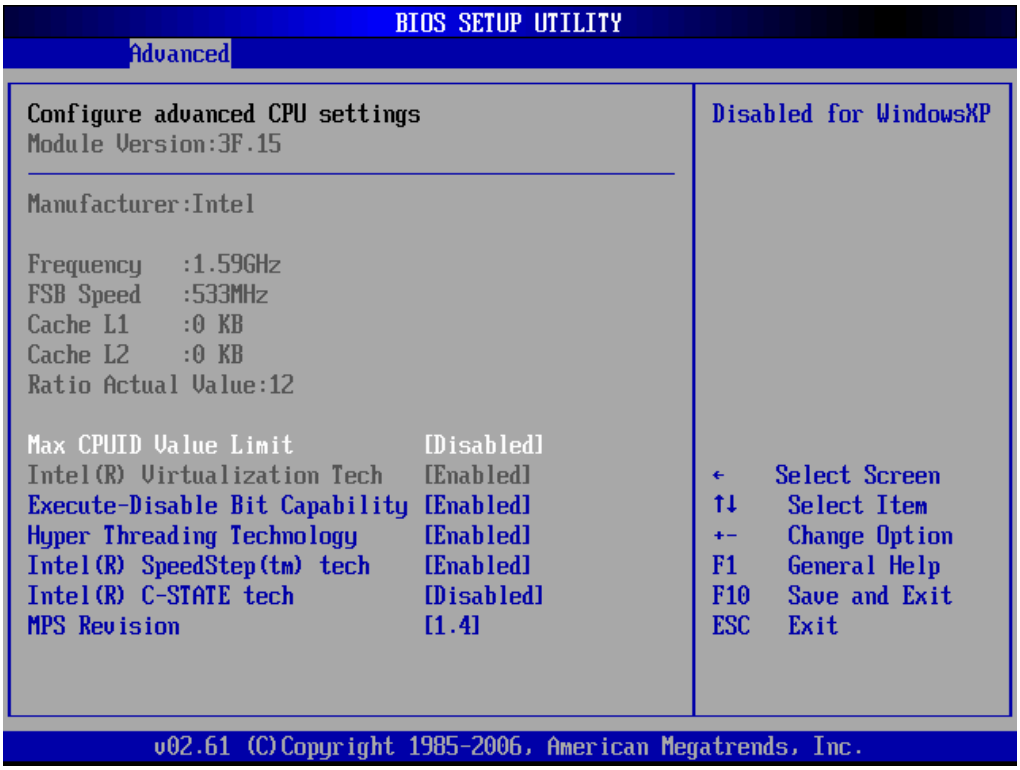


Setting incorrect or conflicting values in Advanced BIOS Setup may cause system malfunctions.

8.3.1 CPU Configuration

CPU Configuration Settings

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *CPU Configuration* screen is shown below.



Max CPUID Value Limit

When the computer is boots, the operating system executes its CPUID instruction to identify the processor and its capabilities. Before it can do so, it must first query the processor to find out the highest input value the CPUID recognizes. This determines the kind of basic information CPUID can provide the operating system. This option allows you to circumvent problems with older operating systems.

When Enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When Disabled, the processor will return the actual maximum CPUID input value of the processor when queried.

Intel® Virtualization Tech

Intel® Virtualization Technology is a set of platform features that supports virtualization of platform hardware and multiple software environmentss. When enabled, it offers data center managers the ability to consolidate multiple workloads on one physical server system.

Execute Disable Bit Capability

This is an Intel hardware-based security feature that can help reduce system exposure to viruses and malicious code. It allows the processor to classify areas in memory where application code can or cannot execute. When a malicious worm attempts to insert code in the buffer, the processor disables its code execution, preventing damage and worm propagation. To use Execute Disable Bit you must have a PC or server with a processor with Execute Disable Bit capability and a supporting operating system.

Hyper-Threading Technology

This option enables/disables Intel® Hyper-Threading Technology.

Intel® SpeedStep tech

This option enables or disables Intel® SpeedStep® technology.

Intel® C-STATE tech

This item allows you to Enable/Disable the C-STATE function. C-STATE make the power and thermal control unit part of the core logic and not part of the chipset as before.

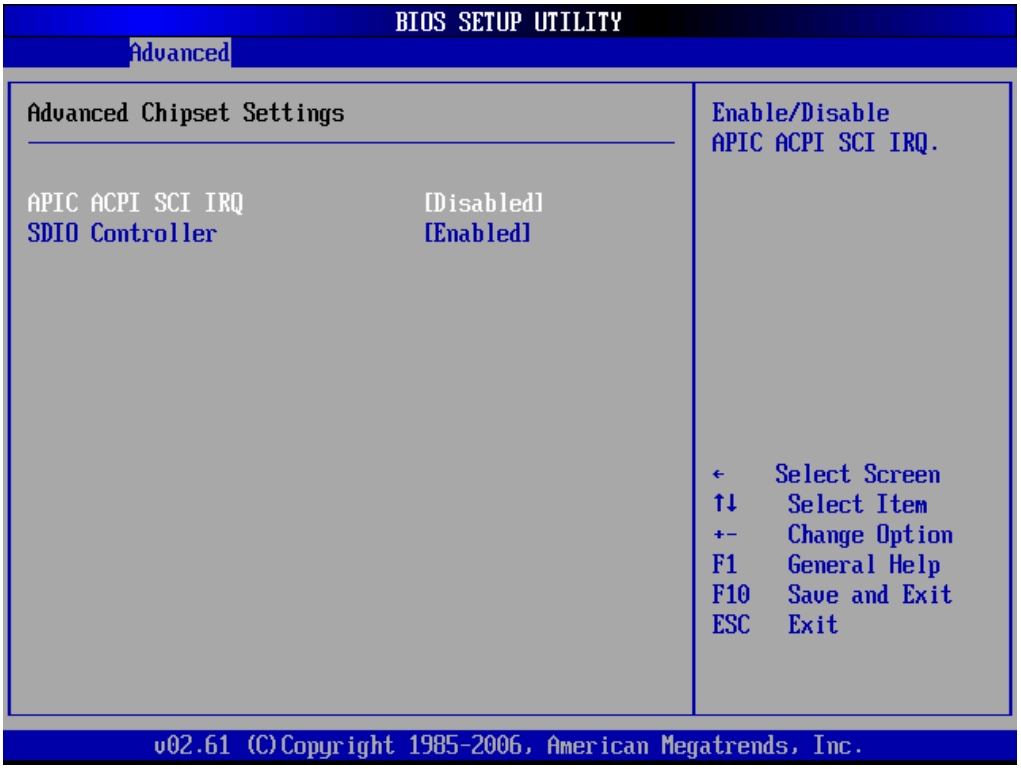
MPS Revision

This item allows you to select which MPS revision to use for the operating system.

8.3.2 Chipset Configuration

Chipset Configuration Settings

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of Chipset BIOS Setup options by highlighting it using the < Arrow > keys. The Chipset BIOS Setup screen is shown below.



APIC ACPI SCI IRQ

This item allows you to enable or disable the APIC ACPI SCI interrupt.

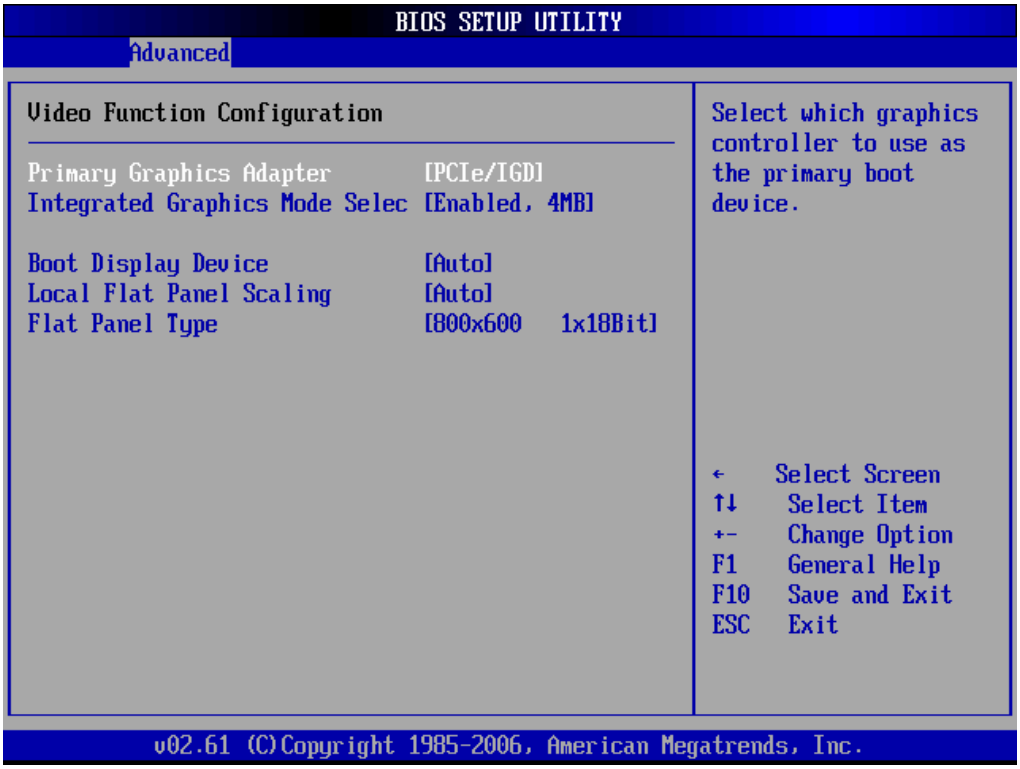
SDIO Controller

This item allows you to enable or disable the internal SD interface controller.

8.3.3 Video Function Configuration

Video Function Configuration Settings

You can use this screen to select options for Video Function configuration settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The video function BIOS Setup screen is shown below.



Primary Graphics Adapter

Selects which graphics controller to use as the primary boot display device. Options: IGD=Integrated Graphic device; PCIe/IGD = first priority is external PCI Express graphics device, secondary is IGD.

Internal Graphics Mode Select

Select amount of system memory which is used by internal graphics device.

Boot Display Device

Selects which display interface you want to make active on boot up.

Local Flat Panel Scaling

Allows you to determine how various resolutions appear on your LCD display.

Auto: The scaling unit on your graphics card will rescale the image before it reaches your LCD display. This option results in the best image quality.

Forced Scaling: This option will maintain the original aspect ratio of the chosen resolution and display it with black bars to the sides/above/below the on-screen image as required.

Disabled: The image isn't scaled at all, but instead your LCD display will run at its maximum resolution and the image will display in the centre of your LCD display. This may result in a black border around the sides of the image.

Flat Panel Type

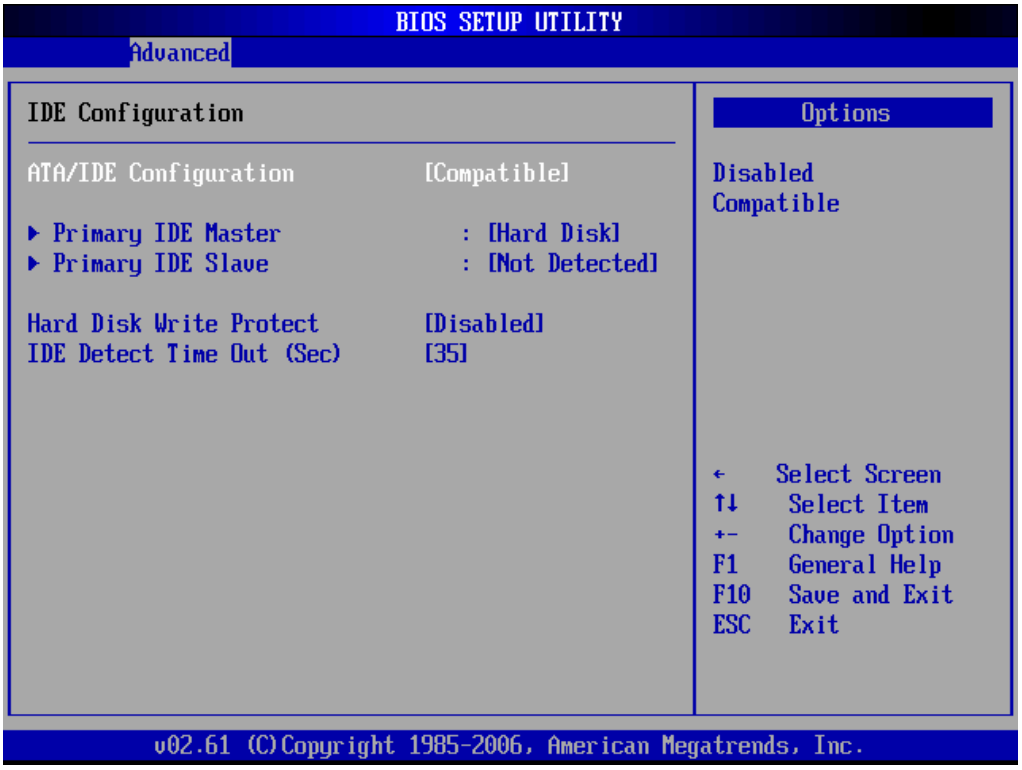
When LVDS is selected from Boot Display Device, this option allows selection of resolution settings for the LVDS interface.

Options: 640x480, 1x18Bit
800x480, 1x18Bit
800x600, 1x18Bit
1024x600, 1x18Bit
1024x768, 1x18Bit
1024x768, 1x24Bit
1280x600, 1x18Bit
1280x768, 1x18Bit
1280x800, 1x18Bit
1366x768, 1x18Bit
1366x768, 1x24Bit

8.3.4 IDE Configuration

IDE Configuration Settings

You can use this screen to select options for the IDE Configuration Settings. An example of the *IDE Configuration* screen is shown below.



ATA/IDE Configuration

This item specifies whether the IDE channels should be initialized in Compatible or Enhanced mode of operation. The settings are Disabled, Compatible and Enhanced.

Primary IDE Master/Slave

Select one of the hard disk drives to configure it. Press < Enter > to access its sub menu.

Hard Disk Write Protect

Set this value to Enabled to prevent the hard disk drive from being overwritten.

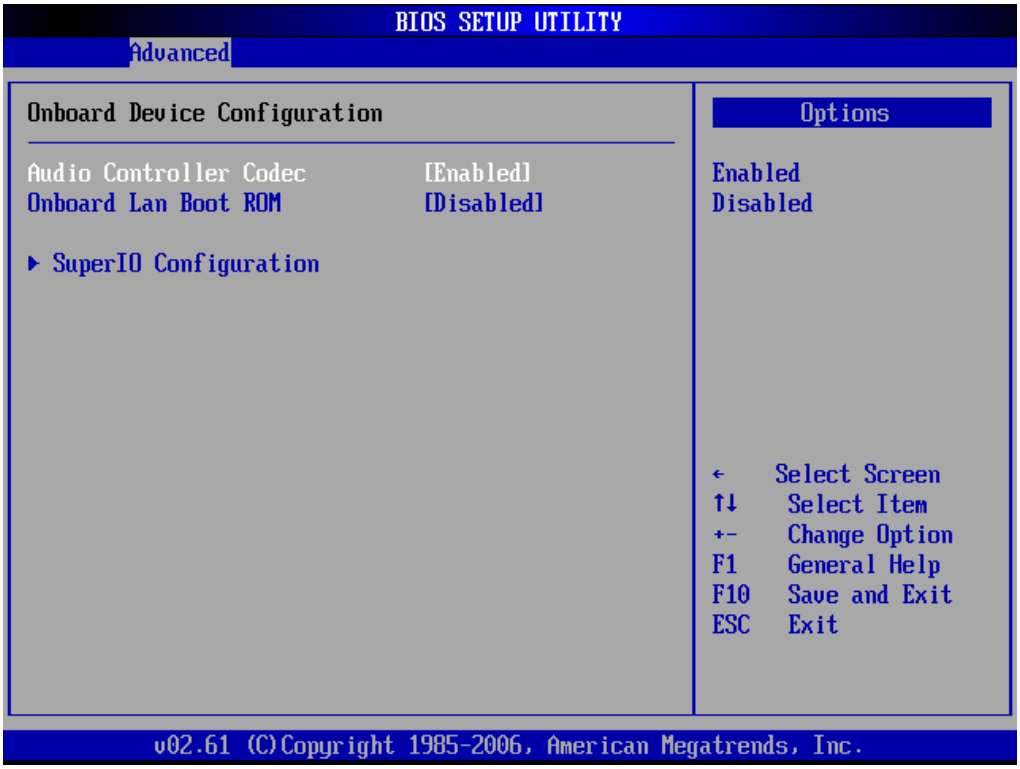
IDE Detect Time Out

This field allows you to set the time to stop searching for IDE devices within the specified number of seconds.

8.3.5 Onboard Device Configuration

Onboard Device Configuration Settings

You can use this screen to specify options for the onboard device configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Audio Controller Codec

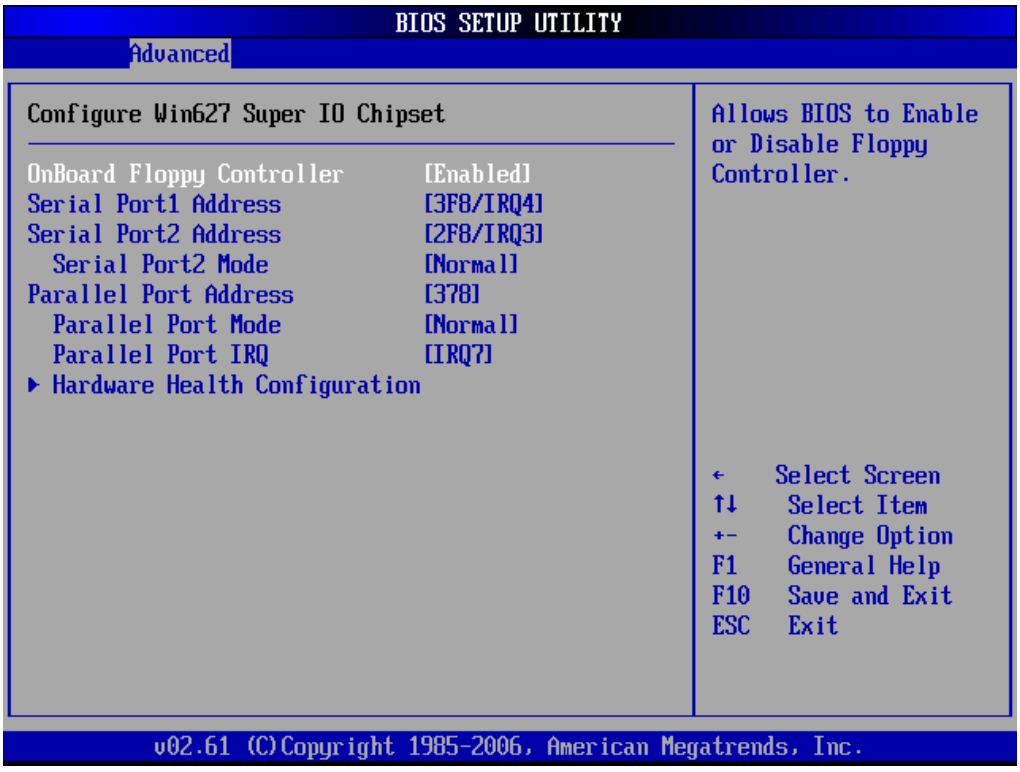
Set this value to Enable/Disable the Audio Controller Codec.

Onboard Lan Boot ROM

Set this value to enable/disable the onboard LAN's PXE ROM to enable boot from LAN. Setting to Disabled can shorten the POST time without initializing LAN PXE ROM if boot from LAN is not needed.

SuperIO Configuration Screen

SuperIO configuration screen is a sub-menu of Onboard Device Configuration. The visibility of this SuperIO configuration screen depends on the presence of an onboard SuperIO (Winbond W83627DHG). If the nanoX-ML is used on carrier w/o a SIO chip, the legacy-free mode will take effect.



OnBoard Floppy Controller

This option enables/disables the Super IO's floppy controller.

Serial Port1 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 1.

Option	Description
Disabled	Set this value to prevent the serial port from accessing any system resources. When this option is set to Disabled, the serial port physically becomes unavailable.
3F8/IRQ4	Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address.
3E8/IRQ4	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address.
2F8/IRQ3	Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address.
2E8/IRQ3	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address.

Serial Port2 Address

This option specifies the base I/O port address and Interrupt Request address of Serial Port2. The settings of Serial Port2 are the same as Serial Port1. However, the setting used by Serial Port1 will not be available for Serial Port2. For example, if Serial Port1 uses 3F8/IRQ4, the option, the 3F8/IRQ4 will not appear in the options of Serial Port2.

Serial Port2 Mode

This option allows the BIOS to select a mode for Serial Port2. The settings are Normal, IrDA, and ASK IR.

Parallel Port Address

This option lets to configure the SuperIO's parallel port address.

Parallel Port Mode

This option specifies the parallel port mode.

Option	Description
Normal	Set this value to allow the standard parallel port mode to be used.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric Bidirectional communication.
EPP+ECP	Allows the parallel port to support both the ECP and EPP modes simultaneously.

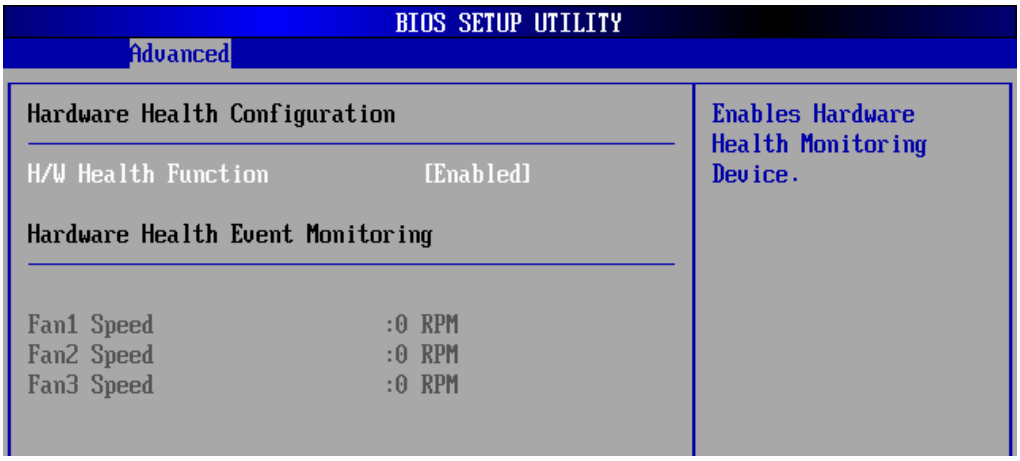
Parallel Port IRQ

This option specifies the IRQ used by the parallel port.

Option	Description
IRQ5	Set this value to allow the serial port to use Interrupt 5.
IRQ7	Set this value to allow the serial port to use Interrupt 7. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.

Hardware Health Configuration

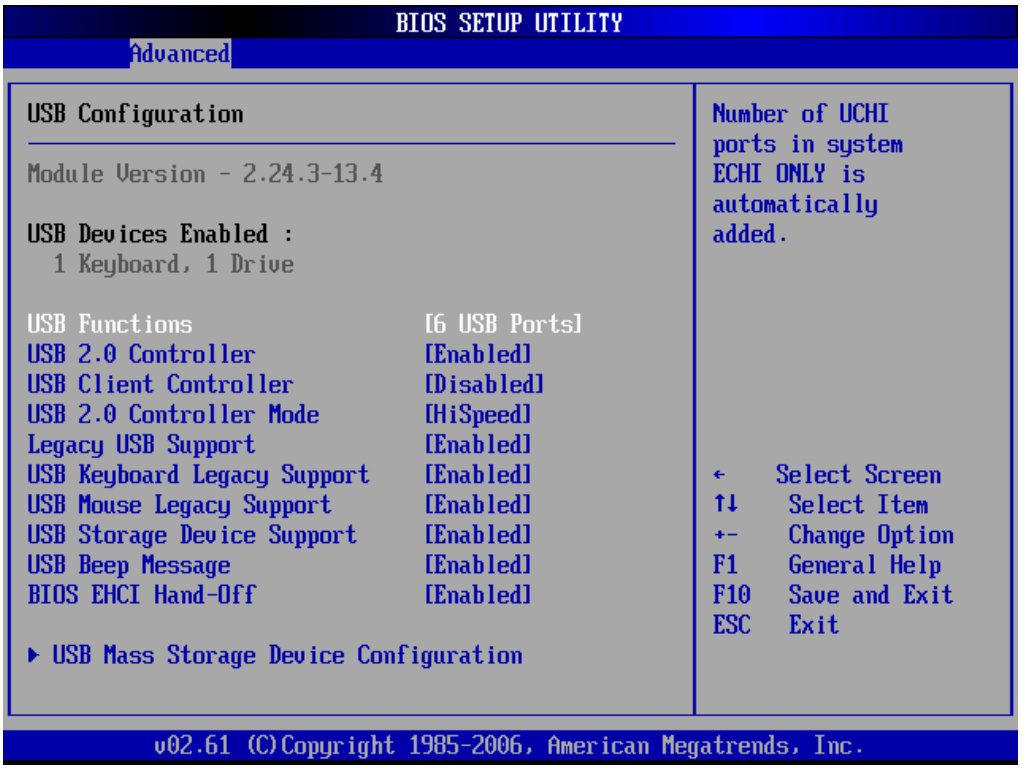
The hardware health function on the SuperIO only supports FAN speed monitoring.



8.3.6 USB Configuration

USB Configuration Settings

You can use this screen to specify options for the USB configuration Settings. The screen is shown below.



USB Function

Set this value to allow the system to Disable, Enable, and select a set number of onboard USB ports.

USB 2.0 Controller

Depends on the setting of USB Function. If USB Function is set to Disabled, this option will have no effect. Enabled will open USB 2.0 functionality to all USB ports.

USB Client Controller Mode

The Intel SCH supports USB client functionality on Port 2 of the USB interface to allow the user to connect to a separate USB host as a peripheral mass storage volume or RNDIS device. This item allows you to enable or disable the USB client function.

USB 2.0 Controller Mode

The USB 2.0 Controller Mode configures the data rate of the USB port. The options are FullSpeed (12 Mbps) and HiSpeed (480 Mbps).

Legacy USB Support

Legacy USB Support refers to USB mouse and keyboard support. Normally if this option is not enabled, any attached USB mouse or keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or keyboard can control the system even when there are no USB drivers loaded on the system. Set this value to enable or disable the Legacy USB Support (see below).

Option	Description
Disabled	Set this value to prevent the use of any USB device in DOS or during system boot.
Enabled	Set this value to allow the use of USB devices during boot and while using DOS.
Auto	This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

USB Beep Message

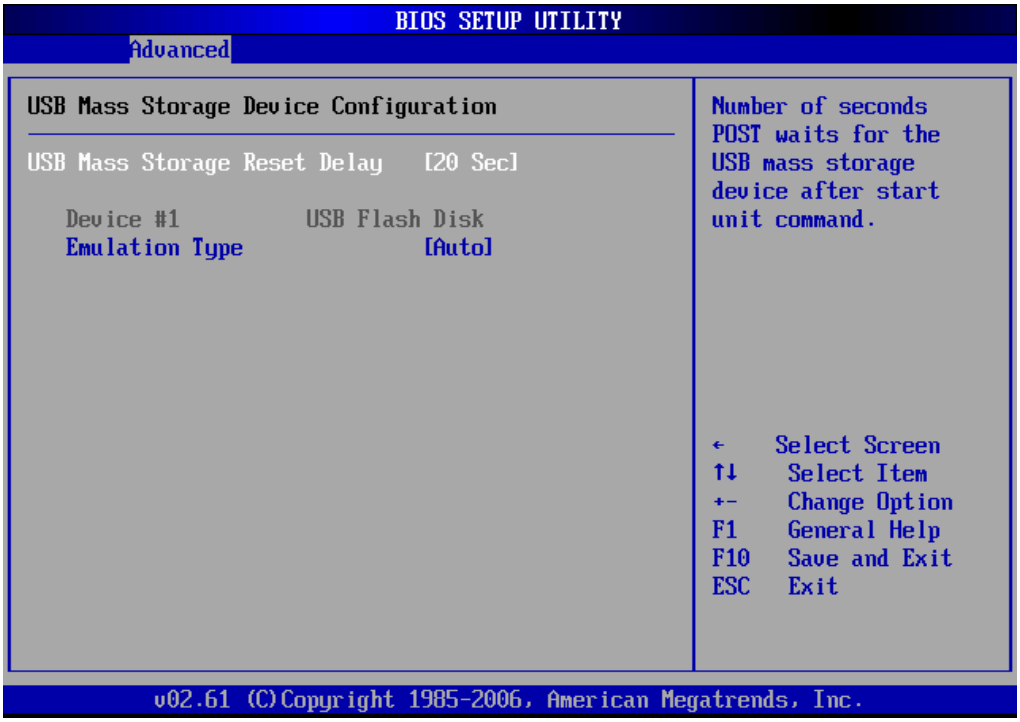
Allows you to Enable/Disable the beep during USB device enumeration.

BIOS EHCI hand-off

This option provides a work around for OSes without ECHI hand-off support. The EHCI ownership change should be claimed by the EHCI driver.

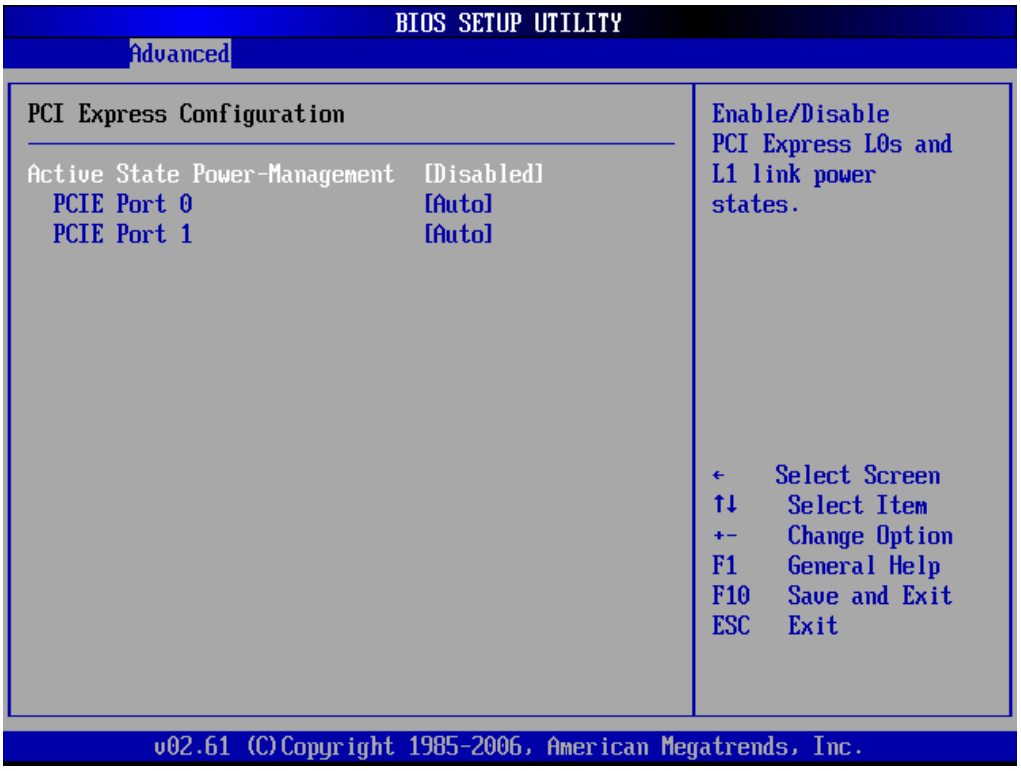
USB Mass Storage Device Configuration

This is a submenu for configuring the USB Mass Storage Class Devices when BIOS finds they are in use on the USB ports. Emulation Type can be set according to the type of attached USB mass storage device(s).). If set to Auto, USB devices less than 530MB will be emulated as Floppy and those greater than 530MB will remain as hard drive. The Forced FDD option can be used to force a hard disk type drive (such as a Zip drive) to boot as FDD.



8.3.7 PCI Express Configuration

You can use this screen to specify options for the PCI Express Configuration Settings.



Active State Power-Management

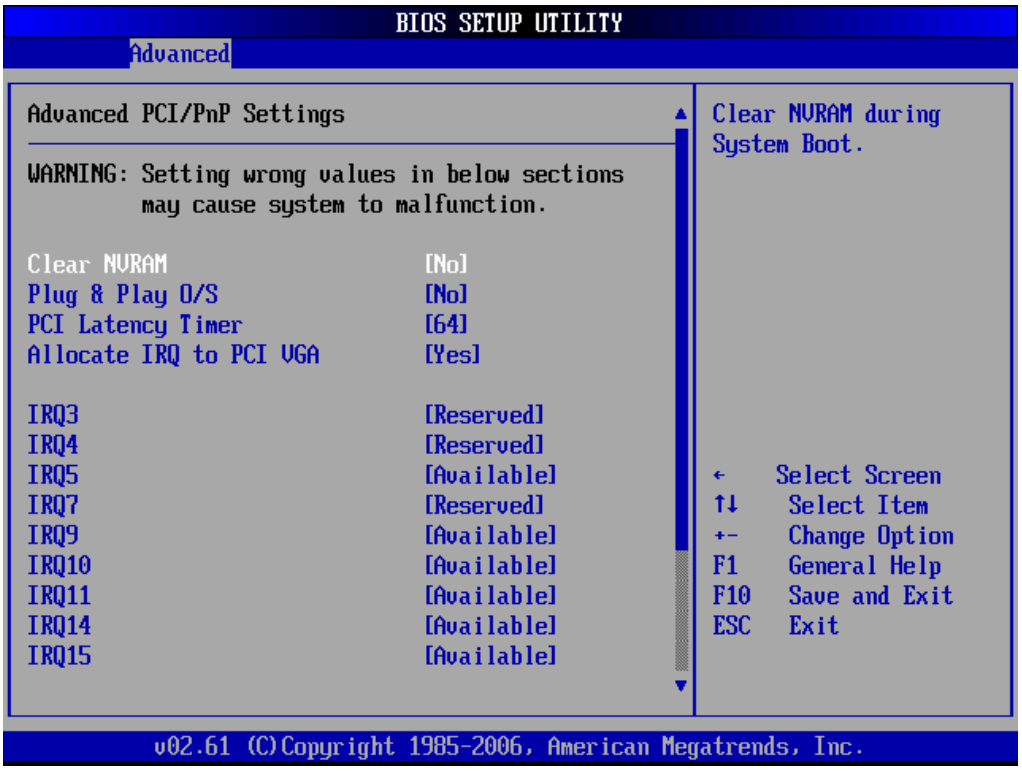
This option allows you to enable/disable the Active State Power Management (ASPM) function. ASPM is a PCIe power management specification.

PCIE Ports 0-1

The options for PCIE Port 0 and 1 are “Auto”, “Enabled”, “Disabled”.

8.3.8 PCIPnP Configuration

You can use this screen to specify options for Plug and Play BIOS Configuration.



Clear NVRAM

This option clears ESCD (Extended System Configuration Data) information in NVRAM.

Plug & Play O/S

When set to "Yes" and a Plug and Play operating system is installed, the operating system configures the Plug and Play devices not required for boot.

PCI Latency Timer

Set this value to allow the PCI Latency Timer to be adjusted. This option sets the latency of all PCI devices on the PCI bus.

Allocate IRQ to PCI VGA

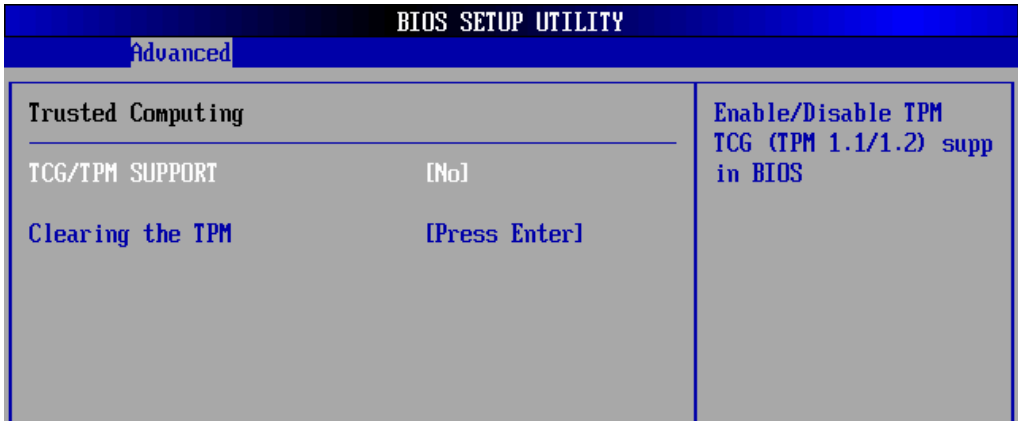
When set to "Yes", the BIOS will assign an IRQ for a PCI VGA card.

IRQ

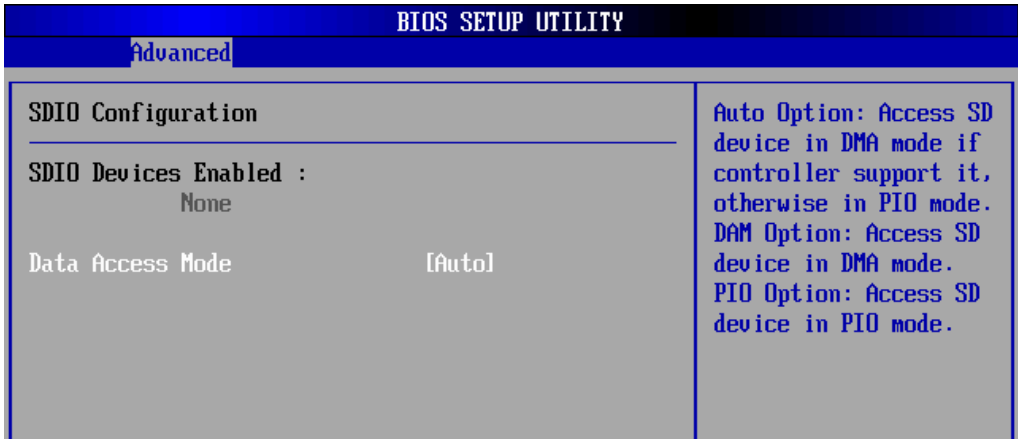
Set this value to allow the IRQ settings to be modified. Available - This setting allows the specified IRQ to be used by a PCI/PnP device. Reserved - This setting allows the specified IRQ to be used by a legacy ISA device.

8.3.9 Trusted Computing

Trusted Computing is NOT supported.



8.3.10 SDIO Configuration



Data Access Mode

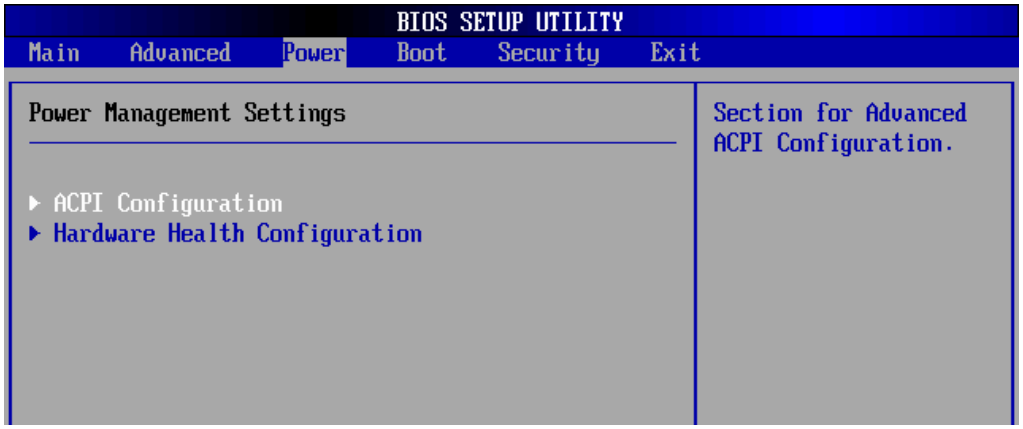
Auto: Access SD device in DMA mode if supported by controller, otherwise use PIO mode.

DMA: Access SD device in DMA mode.

PIO: Access SD device in PIO mode.

8.4 Power Management

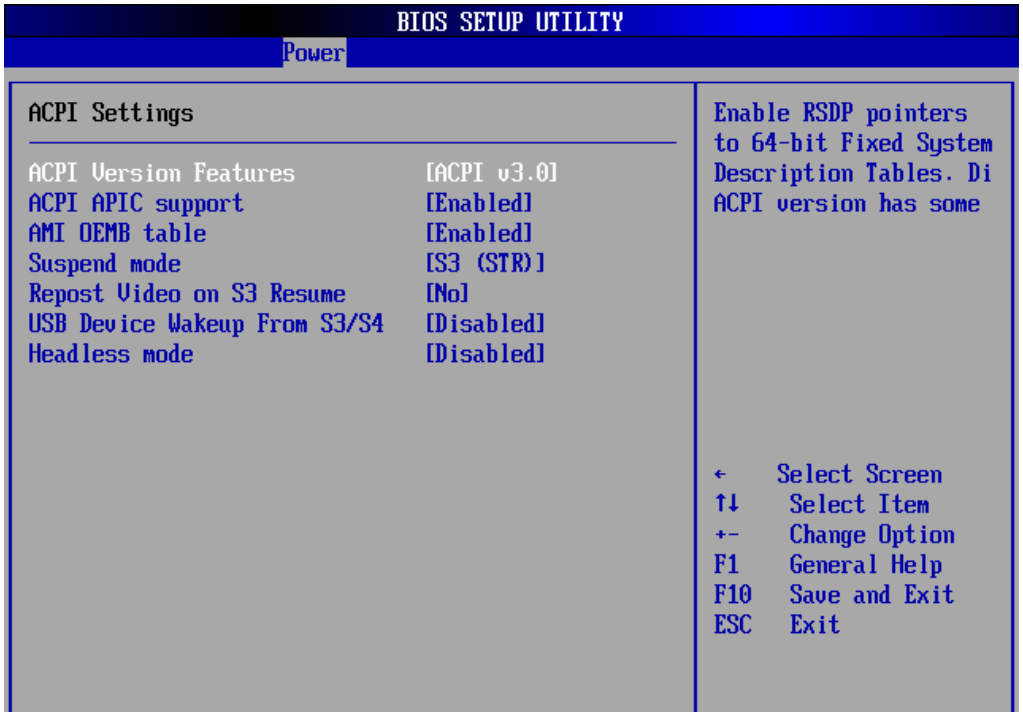
Select the Power tab from the setup screen to enter the power management BIOS Setup screen. The power management BIOS Setup screen is shown below.



8.4.1 ACPI Configuration

Advanced ACPI Configuration

You can use this screen to select options for the ACPI Advanced Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown below.



ACPI Version Features

The item allows you to select the ACPI version.

ACPI APIC Support

Used to enable or disable the Advanced Programmable Interrupt Controller (APIC) for PC2001 compliance. Enabling APIC mode will expand available IRQs resources for the system

AMI OEMB Table

Include OEMB table pointer to R(X)SDT pointer lists.

Suspend mode

This setting selects either *S1 (POS)* or *S3 (STR)* system suspend mode. The Optimal and Fail-Safe Default setting is *S3 (STR)*.

Option	Description
S1 (POS)	Power On Suspend - Under this setting the CPU is not executing instructions, all power resources that supply system level reference of S0 are off, system memory context is maintained, devices that reference power resources that are on are on, and devices that can wake-up the system can cause the CPU to continue to execute from where it left off.
S3 (STR)	Suspend to RAM - Under this setting the system enters a low power state instead of being completely shut off. This allows the computer system to boot up in a few seconds.

Repost Video on S3 Resume

This setting only be visible when suspend mode is set to S3 (STR). It allows the user to select whether or not BIOS performs video initialization after resuming from S3.

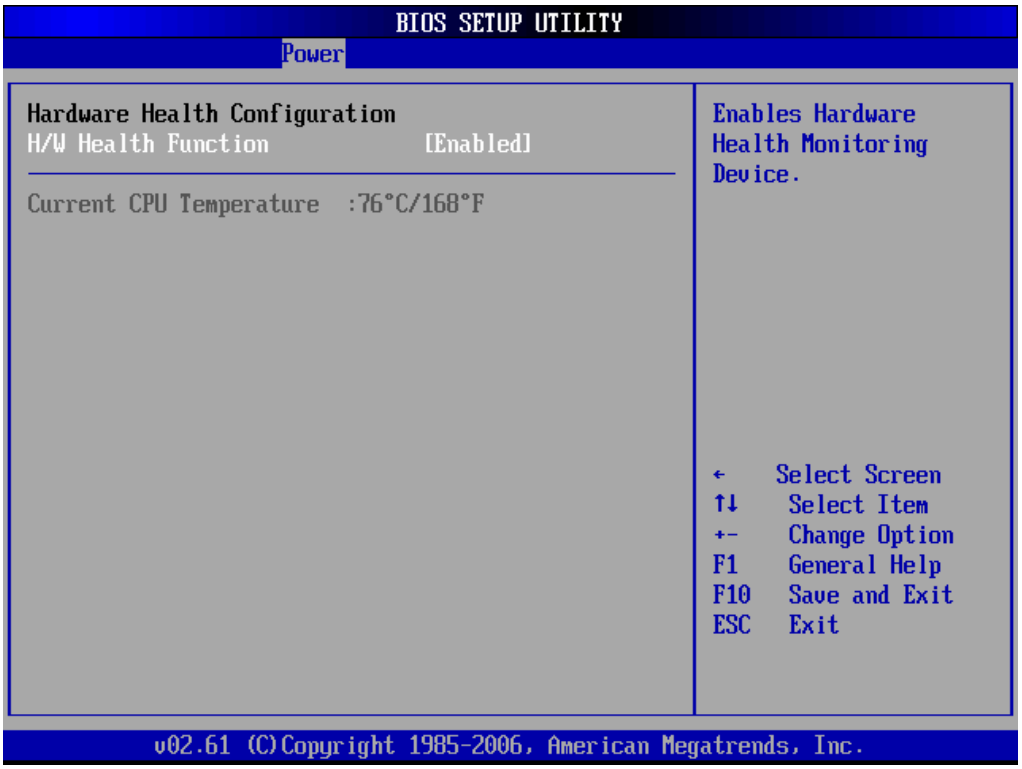
USB Device Wakeup from S3/S4

This option allows a USB device to wake up the system from S3/S4.

Headless mode

This is a server-specific feature. A headless server is one that operates without a keyboard, monitor or mouse. To run in headless mode, both BIOS and operating system (e.g. Windows Server 2003) must support headless operation

8.4.2 Hardware Health Configuration

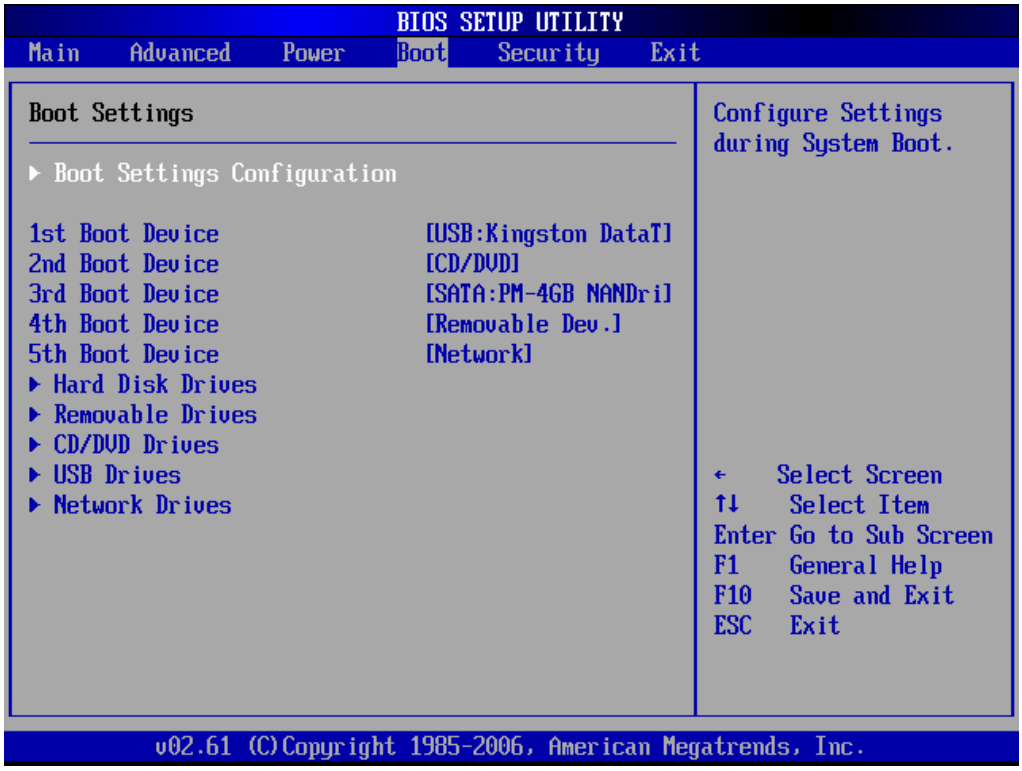


H/W Health Function

This option enables/disables the CPU temperature sensor device on the nanoX-ML.

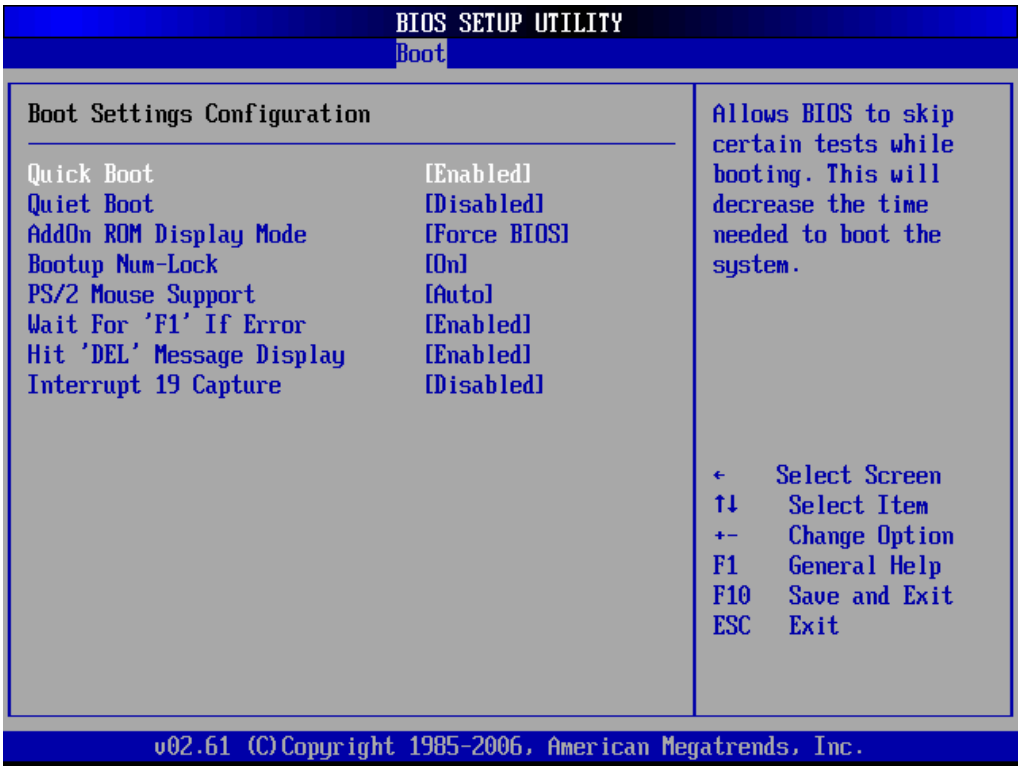
8.5 Boot Setup

Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display an Boot BIOS Setup option by highlighting it using the <Arrow> keys. The Boot Settings screen is shown below:



Boot Settings Configuration

Use this screen to select options for the Boot Settings Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Quick Boot

Disabled - Set this value to allow the BIOS to perform all POST tests.
Enabled - Set this value to allow the BIOS to skip certain POST tests to boot faster.

Quiet Boot

Disabled - Set this value to allow the computer system to display the POST messages.
Enabled - Set this value to allow the computer system to display the OEM logo.

AddOn ROM Display Mode

This BIOS feature controls the display of ROM messages from the BIOS of add-on devices like the graphics card or the SATA controller during the boot sequence. When set to Force BIOS, AddOn ROM messages will be forced to display during the boot sequence. When set to Keep Current, AddOn ROM messages will only be displayed if the third-party manufacturer had set the add-on device to do so.

An AddOn ROM typically consists of firmware that is called by the system BIOS. For example, an adapter card that controls a boot device might contain firmware that is used to connect the device to the system once the AddOn ROM is loaded.

Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up.
Off - This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged.
On - Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

PS/2 Mouse Support

Allows you to Enable/Disable PS/2 mouse support.

Wait for 'F1' If Error

If this option is set to Disabled, AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

When set to Enabled, the system displays the message "Press DEL to run Setup during POST".

Interrupt 19 Capture

Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the AddOn ROM of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's AddOn ROM setup utility, if one is available.

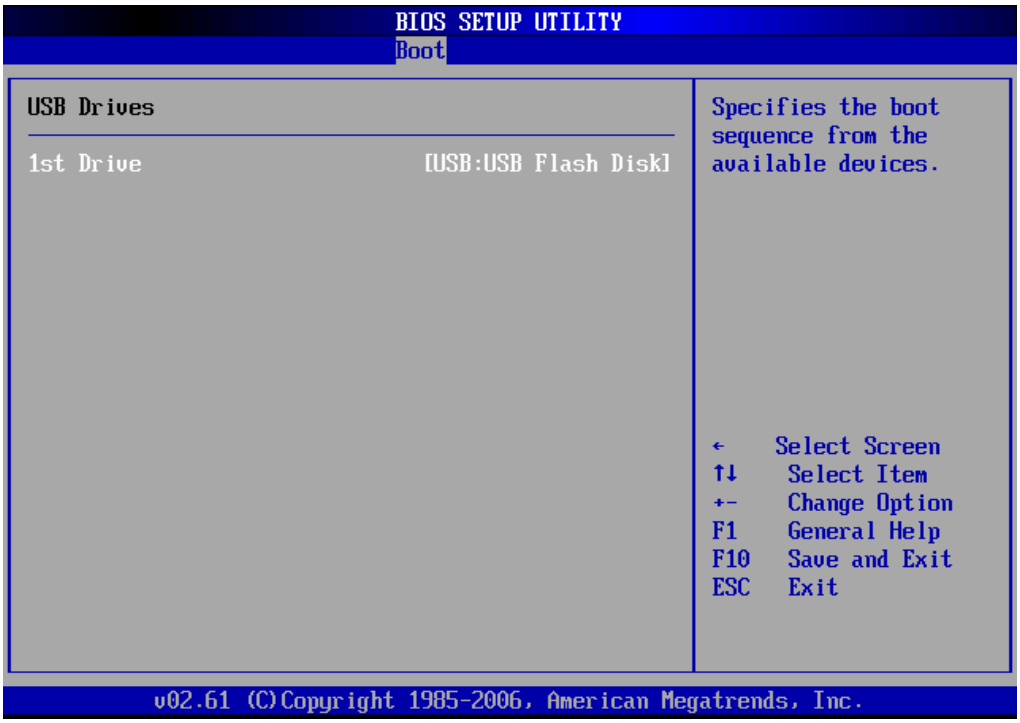
When disabled, the AddOn ROM of these host adaptors will not be able to "capture" interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their AddOn ROM utilities.

Boot Device Priority

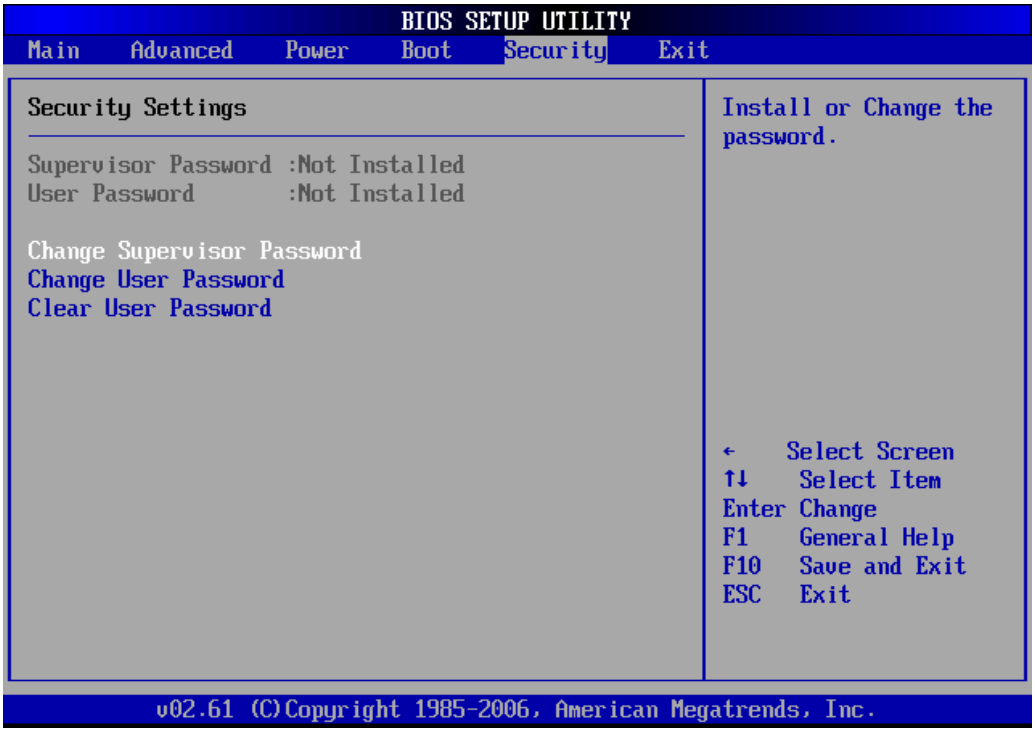
Set the boot device options to determine the sequence in which the computer checks which device to boot from.

Boot Device Groups

The Boot devices are listed in groups by device type. First press <Enter> to enter the sub-menu. Then you may use the arrow keys to select the desired device, then press <+>, <-> or <PageUp>, <PageDown> key to move it up/down in the priority list. For example, USB storage disks will be listed as “USB Drives” in the sub-menu as below. Only the first device in each device group will be available for selection in the Boot Device Priority option.



8.6 Security Setup



8.6.1 Password Support

Two Levels of Password Protection

Provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and re-configure.

Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM.

Select Security Setup from the Setup main BIOS setup menu. Security Setup options, such as password protection and virus protection, are described in this section. To access the sub menu for the following items, select the item and press < Enter >:

- Change Supervisor Password
- Change User Password
- Clear User Password

Supervisor Password

Indicates whether a supervisor password has been set.

User Password

Indicates whether a user password has been set.

Change Supervisor Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the user password.

Clear User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to clear the user password.

8.6.2 Change Supervisor Password

Select Change Supervisor Password from the Security Setup menu and press < Enter >.

```
Enter New Password:
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

8.6.3 Change User Password

Select Change User Password from the Security Setup menu and press < Enter >.

```
Enter New Password:
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

8.6.4 Clear User Password

Select Clear User Password from the Security Setup menu and press < Enter >.

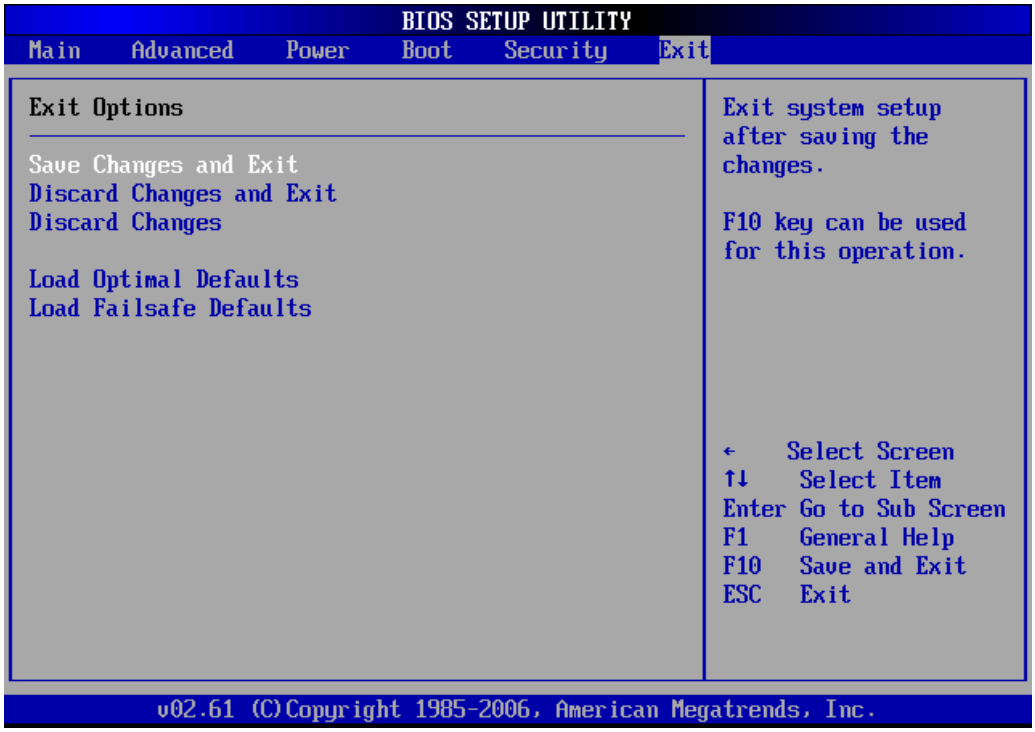
```
Clear New Password

[Ok] [Cancel]
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

8.7 Exit Menu

Select the *Exit* tab from the setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the < Arrow > keys. The Exit BIOS Setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Exit Saving Changes from the Exit menu and press < Enter >.

Save Configuration Changes and Exit Now?

[Ok] [Cancel]

appears in the window. Select Ok to save changes and exit.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration. Select Exit Discarding Changes from the Exit menu and press <Enter>.

Discard Changes and Exit Setup Now?

[Ok] [Cancel]

appears in the window. Select *Ok* to discard changes and exit.

Discard Changes

Select Discard Changes from the Exit menu and press < Enter >.

Select *Ok* to discard changes.

Load Optimal Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Setup options if your computer is experiencing system configuration problems.

Select Load Optimal Defaults from the Exit menu and press < Enter >.

Select *Ok* to load optimal defaults.

Load Failsafe Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Failsafe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe Setup options if your computer is experiencing system configuration problems.

Select Load Fail-Safe Defaults from the Exit menu and press < Enter >.

```
Load Fail-Safe Defaults?

[Ok]    [Cancel]
```

appears in the window. Select Ok to load Fail-Safe defaults.

9 BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMIBIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These are ISA or PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMIBIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMIBIOS checkpoints.

9.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.
DC	System is waking from ACPI S3 state
E1-E8, EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

9.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs From add-in PCI devices.

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

9.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS preboot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs From add-in PCI devices.

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer.Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache – Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.

POST Code Checkpoints cont'd:

Checkpoint	Description
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA...etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Initialization of system management interrupt by invoking all handlers. *Please note this checkpoint comes right after checkpoint 20h*
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

9.4 OEM POST Error Checkpoints

Checkpoints from the range 61h to 70h are reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

9.5 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI- PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble ‘X’ indicates the function number that is being executed. ‘X’ can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
1 = func#1, static devices initialization on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble ‘Y’ indicates the BUS on which the different routines are being executed. ‘Y’ can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = Onboard System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

9.6 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

9.7 Boot Block Beep Codes

No. of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

9.8 POST BIOS Beep Codes

No. of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

9.9 Troubleshooting POST BIOS Beep Codes

No. of Beeps	Description
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. - If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. - If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

Important Safety Instructions

For user safety, please read and follow all instructions, warnings, cautions, and notes marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:

  - Turn off power and unplug any power cords/cables.

- To avoid electrical shock and/or damage to equipment:

  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

- Equipment must be serviced by authorized technicians when:

  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Contact us should you require any service or assistance.

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