NuDAQ® ACL-7122

144-bit Digital I/O Card

User's Manual

Manual Rev. 4.01

Revision Date: December 21, 2006

Part No: 50-11005-101

Recycled Paper

Advance Technologies; Automate the World.

Copyright 2005 ADLINK TECHNOLOGY INC.

All Rights Reserved.

The information in this document is subject to change without prior notice in order to improve reliability, design, and function and does not represent a commitment on the part of the manufacturer.

In no event will the manufacturer be liable for direct, indirect, special, incidental, or consequential damages arising out of the use or inability to use the product or documentation, even if advised of the possibility of such damages.

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

Trademarks

NuDAQ, ACL-LVIEW are trademarks of ADLINK Technology Inc. Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Getting Service from ADLINK

Customer Satisfaction is top priority for ADLINK Technology Inc. Please contact us should you require any service or assistance.

ADLINK TECHNOLOGY INC.

Web Site:	http://www.adlinktech.com
Sales & Service:	Service@adlinktech.com
TEL:	+886-2-82265877
FAX:	+886-2-82265717
Address:	9F, No. 166, Jian Yi Road, Chungho City, Taipei, 235 Taiwan

Please email or FAX this completed service form for prompt and satisfactory service.

Company Information	
Company/Organization	
Contact Person	
E-mail Address	
Address	
Country	
TEL	FAX:
Web Site	
Product Information	
Product Model	
Environment	OS: M/B: CPU: Chipset: BIOS:

Please give a detailed description of the problem(s):

Table of Contents

List of Tables ..... **iii**

List of Figures ..... **iv**

1 Introduction **1**
- 1.1 Features 1
- 1.2 Applications 1
- 1.3 Specifications 2
  - Digital I/O (DIO) 2
  - General Specifications 2
- 1.4 Software Support 3
  - ACLS-DLL1 3
  - ACLS-LVIEW 3

2 Installation **5**
- 2.1 Checklist 5
- 2.2 Unpacking 5
- 2.3 PCB Layout 6
- 2.4 Jumper and DIP Switch Description 7
- 2.5 DIO Numbers Setting 7
- 2.6 Base Address Setting 8
  - How to Define a Base Address for ACL-7122 10
- 2.7 Interrupt Setting 11
  - Summary of Interrupt Status 12
- 2.8 Connector Pin Assignment 14
- 2.9 Connection 16
  - TB-24R, DIN-24R 16
  - TB-24 P, DIN-24P 16
  - TB-16P8R 17
- 2.10 Software Library Installation 17

3 Registers Format 19
3.1 Registers Map 19
3.2 Mode 0 of 8255 PPI 20
3.3 Interrupt Handling 22
Self Interrupt Trigger 23
3.4 Programming Notes 23
3.5 Programming in C language 24

Warranty Policy 29

List of Tables

Table 2-1: 144-bit mode 9
Table 2-2: 96-bit mode 10
Table 2-3: Interrupt Statuses 13
Table 3-1: Ports' I/O Map (Base Address = 2C0H) 19
Table 3-2: Control word (D0 - D4) and mode state (Mode 0 - Mode 15) 21
Table 3-3: Interrupt Trigger Edge 22
Table 3-4: Programmable Mode 22

List of Figures

Figure 2-1: PCB Layout 6
Figure 2-2: SW2 7
Figure 2-3: Default Switch Setting 8
Figure 2-4: JP6 (Default setting IRQ15) 11
Figure 2-5: Block Diagram of Each Channel 14
Figure 2-6: Connector Pin Assignment 15
Figure 3-1: ACL-7122's Signal Direction 23

1 Introduction

ACL-7122 is a 144-channel high-density parallel digital I/O board for ISA bus. This board provides six sets of 24-channel I/O interface. Every 24-channel interface are to emulate mode 1 of the industry standard 8255 Programmable Peripheral Interface (PPI) chips, each offers three 8-bit ports: PA, PB, and PC. PC is subdivided into two nibble-wide (4-bit) ports. Each channel has an individual connector with OPTO-22 pin assignment.

1.1 Features

The ACL-7122 144-Bit Parallel Digital I/O Board provides the following advanced features:

- Compact size (suitable for any size of chassis)
- 144 TTL/DTL compatible digital I/O lines
- Emulates six industry standard mode 0 of 8255 PPI
- Buffered circuits for higher driving
- Direct interface with OPTO-22 compatible I/O module
- Programmable interrupt sources
- Output status read-back
- Fully hardware and software compatible with Advantech PCL-722

1.2 Applications

- High-density programmable mixed digital input and output
- Industrial monitoring and control
- Digital I/O control
- Contact closure, switch/keyboard monitoring
- Connects with OPTO-22 compatible modules

1.3 Specifications

Digital I/O (DIO)

Number of channels:

144 TTL digital compatible inputs and outputs

Input Voltage:

Logic High Voltage: Min. 2.0V, Max. 5.25V

Logic Low Voltage: Min 0.0V, Max. 0.8V

Logic High Current: 22.0uA @ 5V

Logic Low Current: -0.2mA @ 0V

Output Voltage: (Port A and Port B)

Logic High Voltage: Min. 2.4V

Logic Low Voltage: Max. 0.5V

Logic High Current: -2.6mA (current source)

Logic Low Current: 24.0mA (current sink)

Output Voltage: (Port C)

Logic High Voltage: Min. 2.4V

Logic Low Voltage: Max. 0.5V

Logic High Current: -15.0mA (current source)

Logic Low Current: 24.0mA (current sink)

General Specifications

I/O Base Address: 16 consecutive address location

Interrupt IRQ: IRQ 3, 5, 6, 7, 9, 10, 11, 12, 15 (jumper selectable)

Connector: Six 50-pin male ribbon cable connectors

Operating Temperature: 0°C - 55°C

Storage Temperature: -20°C - 80°C

Humidity: 5 - 95%, non-condensing

Power Consumption: +5V @ 1.4A typical, 1.8A maximum

Dimension: 183mm (L) X 119mm

1.4 Software Support

The ACL-7122 is programmed using simple 8-bit I/O port commands. Users can use high level languages, such as BASIC, C, or PASCAL; or low- level languages, such as assembly to program the board. For programming under Windows or LabView, we have ACLS-DLL1 or ACLS-LVIEW available for purchase. Please contact your dealer to purchase. A serial number will be supplied for installing ACLS-DLL1 and ACLS-LVIEW. Without the serial number, the software drivers can still be installed, however your applications would be limited to two hours of operation.

ACLS-DLL1

For easily program the board under Windows environment, we also provide ACLS-DLL1, which include the DLL for Windows 95/98/NT. With ACLS-DLL1, you can use compilers such as VB, VC/C++, or Delphi.

ACLS-LVIEW

For easily link the ACL-7122 with LabView of National Instrument, the ACLS-LVIEW includes the Vis of the ACL-7122 under for Windows 3.1/95/98 and NT.

2 Installation

2.1 Checklist

In addition to this manual, the package includes the following items:

- ACL-7122 144-bit Digital I/O Card
- ADLINK CD

If any of these items are missing or damaged, contact the dealer from whom the product was purchased. Save the shipping materials and carton for storage or future shipping.

2.2 Unpacking

Your ACL-7122 card contains sensitive electronic components that can be easily damaged by static electricity.

The card should be inspected on a grounded anti-static mat. The operator should wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handling damages on the module before proceeding.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface with component side up.

Again inspect the module for damage. Press down on all the socketed IC's to make sure they are properly seated. Do this only with the module placed on a firm flat surface.

Note:	Do not apply power to the card if it has been damaged.

2.3 PCB Layout

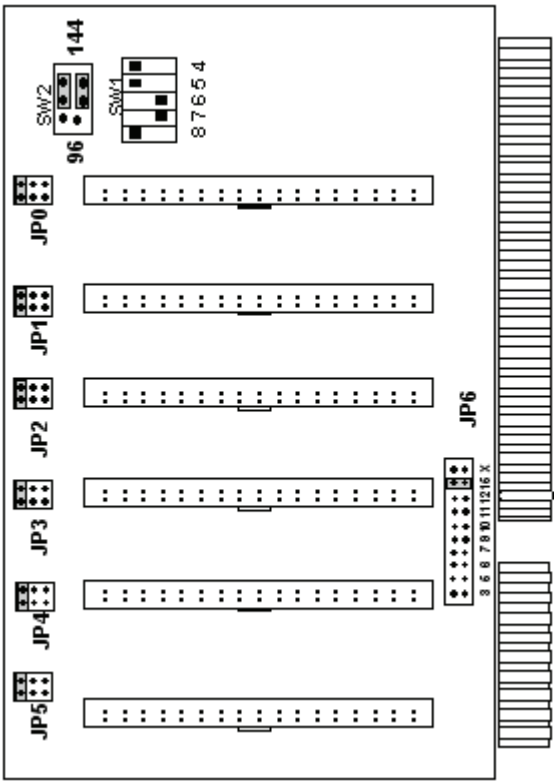


Figure 2-1: PCB Layout

2.4 Jumper and DIP Switch Description

The base address, address parameters, and interrupt can be changed on the ACL-7122 by setting DIP switches and jumpers on the card. The card's jumpers and switches are preset at the factory. Under normal circumstances, there should be no need to change the jumper settings.

A jumper switch is closed (sometimes referred to as "shorted") when the plastic cap is inserted over two pins of the jumper. A jumper is open when the plastic cap is inserted over one or no pin(s) of the jumper.

2.5 DIO Numbers Setting

The ACL-7122 can provide two I/O capability modes: 144-bit and 96-bit. The modes are selected by switch SW2 (see below). The 144-bit mode requires 32 consecutive I/O address. The 96-bit mode just occupies 16 address ports. By default ACL-7122 is set at 144-bit mode. The 96-bit is used only when the address conflicts with the address of other I/O cards.

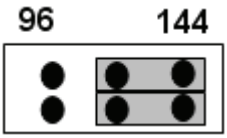


Figure 2-2: SW2

Note:	In 96-bit mode, two or more boards can be mapped consecutively on adjacent addresses. However, under 144-bit mode, each board should have a gap of eight addresses.

2.6 Base Address Setting

ACL-7122 requires 32 or 16 consecutive address locations in I/O address space. The base address of the ACL-7122 is restricted by the following conditions.

1. The base address must be within the range of 200hex and 3FFhex.
2. The base address should not be in conflict with any PC reserved I/O address or other I/O cards' address.

The ACL-7122 requires 32 consecutive address locations for 144-bit mode, or 16 address locations for 96-bit mode. The I/O port base address is selectable by a five position DIP switch SW1 (refer to Figure 2-3). The address setting of 144-bit mode for I/O port from hex200 to hex3FE is described in Table 2-1. The address setting of 96-bit mode is described in Table 2-2.

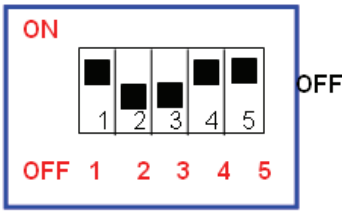


Figure 2-3: Default Switch Setting

I/O port address(hex)	1 A8	2 A7	3 A6	4 A5	5 A4
200-21F	ON (0)	ON (0)	ON (0)	ON (0)	X
:					
(*) 2C0-2DF (default setting)	ON (0)	OFF (1)	OFF (1)	ON (0)	X
:					
380-39F	OFF (1)	OFF (1)	ON (0)	ON (0)	X
3A0-3BF	OFF (1)	OFF (1)	ON (0)	OFF (1)	X
3C0-3DF	OFF (1)	OFF (1)	OFF (1)	ON (0)	X
3E0-3FF	OFF (1)	OFF (1)	OFF (1)	OFF (1)	X

Table 2-1: 144-bit mode

Legend:

X: Irrelevant. Either ON = 0 or OFF = 1 can be used.

A2,..., A8 correspond to address lines of ISA bus.

A9 is always 1 (OFF).

Note: In 144-bit mode, either setting can be used in the base address line A4.

I/O port Address(hex)	1 A8	2 A7	3 A6	4 A5	5 A4
200-20F	ON	ON	ON	ON	ON
:					
290-29F	ON	OFF	ON	ON	OFF
2A0-2AF	ON	OFF	ON	OFF	ON
:					
3D0-3DF	OFF	OFF	OFF	ON	OFF
3E0-3EF	OFF	OFF	OFF	OFF	ON
3F0-3FF	OFF	OFF	OFF	OFF	OFF

Table 2-2: 96-bit mode

How to Define a Base Address for ACL-7122

DIP1 to DIP6 in switch SW1 correspond one to one with the PC bus address line A9 to A4. A9 is always 1; A3 to A0 are always 0 with hardware. To change the base address, only the values from A8 to A4 can be changed (shaded area in diagram below). The example below illustrates how to define the base address as Hex 2C0.

Base Address: Hex 2C0

2		**C**				**0**			
1	0	1	1	0	0	0	0	0	0
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OFF	ON	OFF	OFF	ON	ON				

2.7 Interrupt Setting

ACL-7122 provides nine interrupt requests levels (IRQ) 3, 5, 6, 7, 9, 10, 11, 12, and 15. The IRQ level is set by jumper JP6. The IRQ signal is Tri-state allowing multiple ACL-7122 boards to share the same interrupt line. For example, two ACL-7122 can share IRQ 3 in one system.

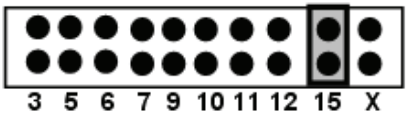


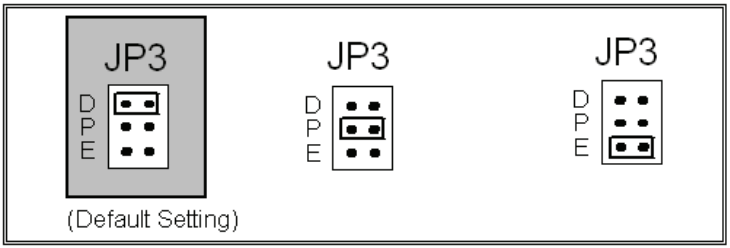
Figure 2-4: JP6 (Default setting IRQ15)

The ACL-7122 has two lines (PC0 and PC3) to generate hardware interrupt. The interrupt are edge-triggered, PC0 traps a rising edge signal, while PC3 traps a falling edge signal.

To use the interrupt, select the IRQ interrupt level. To determine which input to generate the interrupt, you can read Port C, bit PC-0, and bit PC-3 to locate the current state of inputs.

Note:	Input is not latched and no first event trapping is provided to determine which input was active first.

There are six jumpers from JP0 to JP5, which corresponds to each channel in ACL-7122, for interrupt enabled selection. The figure below illustrates the three statuses of interrupt setting for CH3.



Legend:

D: Disabled Interrupt - No interrupt request

P: Programmable Interrupt - interrupt when CH3‘s PC4 is “Low”

E: Enable Interrupt - interrupts request

Summary of Interrupt Status

In ACL-7122, the interrupt trigger source is depended on jumpers J0 to J5, and, I/O lines, PC0, PC3, and PC4. All possible interrupt statuses are shown in the following table.

JPn (n=0...5)	PC0	PC3	PC4	Interrupt Status
	X	X	X	No Interrupt Request
	LOW	L -> H	LOW	Interrupt Request
	L ->H	HIGH	LOW	
	HIGH	X	LOW	No Interrupt Request
	X	LOW	LOW	
	X	X	HIGH	No Interrupt Request
	HIGH	X	X	No Interrupt Request
	X	LOW		
	LOW	L -> H	X	Interrupt Request
	L -> H	HIGH		

Table 2-3: Interrupt Statuses

X: Irrelevant, can be set at any value.

H -> L: Rising Edge Trigger (from High to Low)

L -> H: Falling Edge Trigger (from Low to High)

2.8 Connector Pin Assignment

The I/O ports of ACL-7122 emulate six mode 0 of Intel 8255 general purpose programmable peripheral interface. Figure 2-5 shows ACL-7122's equally block diagram of each channel. Six 50-pin connectors come equipped with the ACL-7122 board with each of them corresponding to a mode 0 of 8255. The connector pin assignment is specified in Figure 2-6.

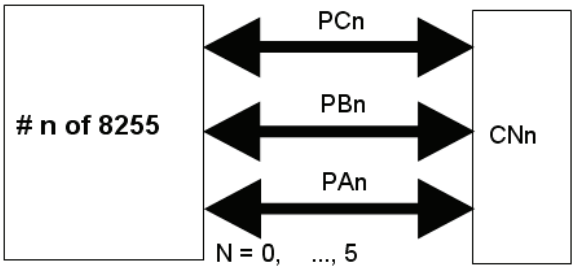


Figure 2-5: Block Diagram of Each Channel

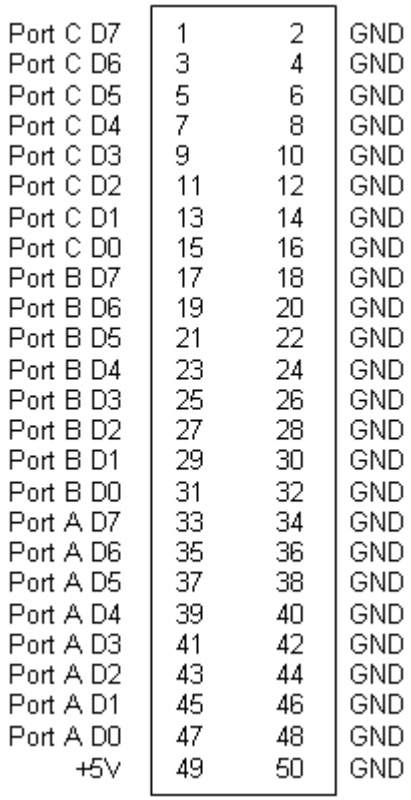


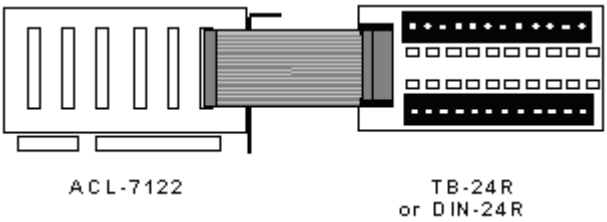
Figure 2-6: Connector Pin Assignment

2.9 Connection

There are three daughter boards to connect with ACL-7122 for DIO operation. The following diagrams illustrate the configuration of ACL-7122 with different terminal boards.

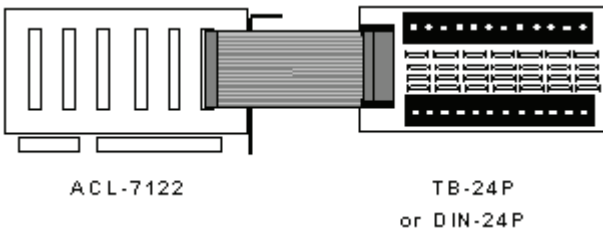
TB-24R, DIN-24R

TB-24R and DIN-24R provide 24 Form C relays for digital output control. The connection between ACL-7122 and TB-24R is:



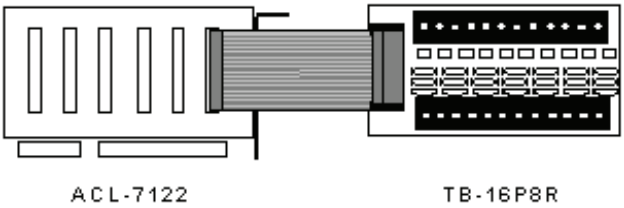
TB-24 P, DIN-24P

TB-24P and DIN-24P provide 24 opto-isolated digital input channels, the connection between ACL-7122 and TB-24P is:



TB-16P8R

TB-16P8R provides 16 opto-isolated digital input channels and eight relay outputs, the connection between ACL-7122 and TB-16P8R is:



2.10 Software Library Installation

This section describes the DOS software library, which is supplied free of charge. The function prototypes and some useful constants are defined in the header files in the LIB directory. The DOS library software includes a utility program, C language library, and some demonstration programs, which can reduce the amount of programming required. Please refer to the ACLS-DLL1 function reference manual included in the ADLINK CD. The DOS functions are compatible with ACLS-DLL1 functions except without a “W” prefix in function names.

To program in a Windows environment, please use ACLS-DLL1, which requires a license.

To install the DOS library software and utilities, follow the instructions below:

1. Insert the ADLINK CD into the appropriate CD-ROM drive.
2. Type the following command (X indicates the CD-ROM drive): **X:\>CD\NuDAQISA\7122**
3. Execute the setup batch program to install the software: **X:\NuDAQISA\7122>SETUP**

After installation, all files in ACL-7122 Library & Utility for DOS are stored in C:\ADLINK\7122\DOS sub-directory.

3 Registers Format

3.1 Registers Map

ACL-7122 needs 24 bytes of I/O address to operate. The relationship between the I/O address and ports' data read/write is shown in the table below, using the default base address of 2C0H.

Port Select	Address	Note
CH0 PA0	2C0H	EMULATE 8255 PA
CH0 PB0	2C1H	EMULATE 8255 PB
CH0 PC0	2C2H	EMULATE 8255 PC
CONTROL WORD CH0	2C3H	EMULATE 8255 CW
CH1 PA1	2C4H	EMULATE 8255 PA
CH1 PB1	2C5H	EMULATE 8255 PB
CH1 PC1	2C6H	EMULATE 8255 PC
CONTROL WORD CH1	2C7H	EMULATE 8255 CW
CH2 PA2	2C8H	EMULATE 8255 PA
CH2 PB2	2C9H	EMULATE 8255 PB
CH2 PC2	2CAH	EMULATE 8255 PC
CONTROL WORD CH2	2CBH	EMULATE 8255 CW
CH3 PA3	2CCH	EMULATE 8255 PA
CH3 PB3	2CDH	EMULATE 8255 PB
CH3 PC3	2CEH	EMULATE 8255 PC
CONTROL WORD CH3	2CFH	EMULATE 8255 CW
CH4 PA4	2D0H	EMULATE 8255 PA
CH4 PB4	2D1H	EMULATE 8255 PB
CH4 PC4	2D2H	EMULATE 8255 PC
CONTROL WORD CH4	2D3H	EMULATE 8255 CW
CH5 PA5	2D4H	EMULATE 8255 PA
CH5 PB5	2D5H	EMULATE 8255 PB
CH5 PC5	2D6H	EMULATE 8255 PC
CONTROL WORD CH5	2D7H	EMULATE 8255 CW

Table 3-1: Ports' I/O Map (Base Address = 2C0H)

Port Select	Address	Note
--	2D8H	Reserved by ACL-7122
--	2D9H	Reserved by ACL-7122
--	2DAH	Reserved by ACL-7122
--	2DBH	Reserved by ACL-7122
--	2DCH	Reserved by ACL-7122
--	2DDH	Reserved by ACL-7122
--	2DEH	Reserved by ACL-7122
--	2DFH	Reserved by ACL-7122

Table 3-1: Ports' I/O Map (Base Address = 2C0H)

3.2 Mode 0 of 8255 PPI

ACL-7122 emulates MODE 0 of 8255 PPI, and comes equipped with six 50-pin male IDC connectors that interface with OPTO-22 racks 8, 16, and 24.

The basic function definitions of 8255 mode 0 are:

- Two 8-bit I/O ports - PA and PB
- Two nibble-wide (4-bit) ports - PC upper and PC lower
- Any ports can be used for both input and output
- Outputs are latched whereas inputs are not latched

Two of the I/O lines (PC-0, PC-3) of each channel can be used to generate a hardware interrupt.

The control word is used to program PA, PB and PC as input port or output port. The following table summarizes the control word (D0 - D4) and the corresponding mode state (Mode 0 - Mode 15).

Mode	Config. Value	D4	D3	D1	D0	Port A	Port C Upper	Port B	Port C Lower
0	80H	0	0	0	0	O/P	O/P	O/P	O/P
1	81H	0	0	0	1	O/P	O/P	O/P	I/P
2	82H	0	0	1	0	O/P	O/P	I/P	O/P
3	83H	0	0	1	1	O/P	O/P	I/P	I/P
4	88H	0	1	0	0	O/P	I/P	O/P	O/P
5	89H	0	1	0	1	O/P	I/P	O/P	I/P
6	8AH	0	1	1	0	O/P	I/P	I/P	O/P
7	8BH	0	1	1	1	O/P	I/P	I/P	I/P
8	90H	1	0	0	0	I/P	O/P	O/P	O/P
9	91H	1	0	0	1	I/P	O/P	O/P	I/P
10	92H	1	0	1	0	I/P	O/P	I/P	O/P
11	93H	1	0	1	1	I/P	O/P	I/P	I/P
12	98H	1	1	0	0	I/P	I/P	O/P	O/P
13	99H	1	1	0	1	I/P	I/P	O/P	I/P
14	9AH	1	1	1	0	I/P	I/P	I/P	O/P
15	9BH	1	1	1	1	I/P	I/P	I/P	I/P

Table 3-2: Control word (D0 - D4) and mode state (Mode 0 - Mode 15)

3.3 Interrupt Handling

ACL-7122 can generate a hardware interrupt to your PC. The following issues should be careful when you want to generate an interrupt trigger.

1. Interrupt IRQ level setting: make sure the right IRQ level is set by using jumper J6.
2. Interrupt trigger status setting:

- Interrupt Mode: make sure jumper J2 is already set as E(Enable) or P(PMG) mode.
- Interrupt Trigger Edge: if E mode is chosen, take note of the following combinations of PC-0 and PC-3:

PC0	PC3	Status
High	X	No Interrupt Request
Low	Low >> High	Interrupt Request
X	Low	No Interrupt Request
Low >> High	High	Interrupt Request

Table 3-3: Interrupt Trigger Edge

X: Irrelevant - any value can be set

- Programmable Mode: If in P mode, ensure that the I/O line PC-4 is kept in TTL LOW status. Otherwise, no interrupt trigger will occur. The relationships between PC4, PC3, and PC0 are as follows:

PC4	PC0	PC3	Status
Low	High	X	No Interrupt Request
	Low	Low >> High	Interrupt Request
	X	Low	No Interrupt Request
	Low >> High	High	Interrupt Request
High	X	X	No Interrupt Request

Table 3-4: Programmable Mode

X: Irrelevant - any value can be set

Note:	ACL-7122's input is not latched and no first event trapping is provided to determine which input was active first.

Self Interrupt Trigger

Although ACL-7122's interrupt signals are normally received from external peripherals. It can also generate a test output signal to emulate an interrupt being inputted from an external device.

3.4 Programming Notes

Before programming ACL-7122, the following notes might be useful in controlling the I/O operations through ACL-7122.

- Default Input Mode

  After power-on or hardware reset of your PC system, all ports of ACL-7122 are automatically configured as INPUT mode.

- Output Latch

  When an output port is programmed as output mode through control word, it will not affect the connected output device until an output instruction is executed. This means there will be no data output until the first O/T instruction is executed.

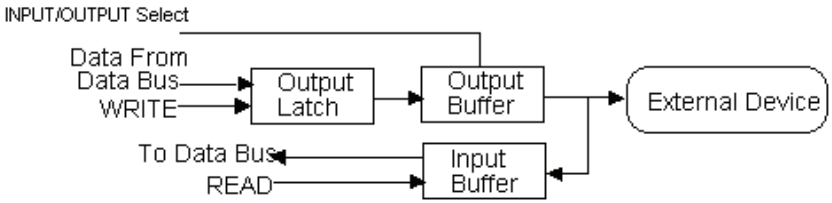


Figure 3-1: ACL-7122's Signal Direction

- In reference to the above ACL-7122's signal direction block diagram above, the following points should be noted:
  - When a port is set as INPUT or after hardware RESET, its output buffer is Disabled (high impedance)
  - The output data is lactated in the Output Latch when it is set as OUTPUT mode.
  - When the port is set as OUTPUT, the input circuit is used as an output status read-back.
  - The data in Output Latch is a random value after power on. It has to be initialized before the port to output direction.

3.5 Programming in C language

The following are examples written in C language. The first four parts are only partial programs for your reference; you can not compile them before these programs are complete.

The last program is an example for interrupt handling, you could compile it by Borland C/C++ compiler directly.

1. To initial I/O port

```
# define BASE 0x2C0          //define base address
# define CWD0 0x80           //XX refer to 8255 CW
int i;

for( i = 0 ; i < 6; i++)
{
    outportb( BASE + i * 4 + 0 , 0x00);
    outportb( BASE + i * 4 + 1 , 0x00);
    outportb( BASE + i * 4 + 2 , 0x00);
    outportb( BASE + i * 4 + 3 , CWD);
/* all as output */
}
```

2. To write port

```
# define BASE 0x2C0          //define base address
# define PA   0x0            // Port A
# define PB   0x1            // Port B
# define PC   0x2            // Port C
# define CWD 0x80            //ALL output to 8255 CW

outportb(BASE + 3,CWD);      //index to CH0 CW
outportb(BASE + PA ,0x23); // write 23H to CH0 PA
outportb(BASE + PB ,0x45); // write 45H to CH0 PA
outportb(BASE + PC ,0xfd); // write fdH to CH0 PA
```

3. To access port

```
# define BASE 0x2C0          //define base address
# define PA   0x0            // Port A
# define PB   0x1            // Port B
# define PC   0x2            // Port C
# define CWD 0x9B           //ALL input from 8255 CW
int pa_data, pb_data, pc_data;

outportb(BASE + 3,CWD);      //index to CH0 CW
pa_d = inportb(BASE + PA); // read from CH0 PA
pb_d = inportb(BASE + PB); // read from CH0 PB
pc_d = inportb(BASE + PC); // read from CH0 PC
```

4. To clear and enable interrupt

```
# define INDEX 0x2C0     //INDEX same as SW
                         //setting
# define DATAS 0x301     //data R/W port
# define CW1 0x3         //8255 port 0 CW index
int dummy;               //dummy data buffer
outportb(INDEX,CW1);     //index to CW
dummy = inportb(DATA);   //dummy read to clear
                         //and enable interrupt
```

5. A Complete Sample Program for Interrupt Handling

```
/*****************************************************/
 *  This program deno. how to generate interrupt by *
 *  the ACL-7122 itself. When you press any key, a  *
 *  beep is generated. When you press ESC key, the  *
 *  system will be quit.                            *
 *                                                  *
 *  Hardware setting :                              *
 *     Base Address : 0x2C0                         *
 *     IRQ Level    : 9    ( Jumper J6)             *
 *     Int mode     : P   ( jumper J0)               *
 *     edge trigger : PC3 0->1 ( rising edge)        *
 *****************************************************/


#include <stdio.h>
#include <dos.h>
#include <conio.h>

#define  IRQ2        0x0a
#define  EOI         0x20
#define  BASE_ADDR   0x2c0
#define  PA          0x00
#define  PB          0x01
#define  PC          0x02
#define  CW          0x03

void interrupt isr_7122()
{
    printf("\7");             // beep
    outportb( 0x20, EOI);     // EOI of 8259
}
main()
{
    int  mask, keyin;
    void interrupt (*old_irq2_isr)();

    old_irq2_isr = getvect( IRQ2);
```

```
    setvect( IRQ2, isr_7122);
    mask = inportb( 0x21);

    outportb(BASE_ADDR + CW, 0x80); // set PA, PB and
PC
                                    // as output mode
    clrscr();                       // clear screen
    printf( " press <ESC> to QUIT \n");
    do
    {
       keyin = 0;
       printf(" press any key to generate an interrupt
                except <ESC>\n");
       keyin = bioskey(0);

       outportb( 0x21, 0xbf & mask); // IRQ2 nonmasked

       outportb( BASE_ADDR + PC, 0x00);
       delay( 100);
       outportb( BASE_ADDR + PC, 0x08);

     } while( (keyin & 0xff) != 27); // QUIT when ESC
pressed

    setvect( IRQ2, old_irq2_isr); // restore old isr
    outportb( 0x21, mask);        // restore 8259 mask}
```

Warranty Policy

Thank you for choosing ADLINK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ADLINK's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: http://rma.adlinktech.com/policy/.
2. All ADLINK products come with a limited two-year warranty, one year for products bought in China:
   - The warranty period starts on the day the product is shipped from ADLINK's factory.
   - Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.
   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for any loss of data.
   - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
   - For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.

3. Our repair service is not covered by ADLINK's guarantee in the following situations:
   - Damage caused by not following instructions in the User's Manual.
   - Damage caused by carelessness on the user's part during product transportation.
   - Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
   - Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
   - Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - Damage from improper repair by unauthorized ADLINK technicians.
   - Products with altered and/or damaged serial numbers are not entitled to our service.
   - This warranty is not transferable or extendible.
   - Other categories not protected under our warranty.
4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website: http://rma.adlinktech.com/policy. Damaged products with attached RMA forms receive priority.

If you have any further questions, please email our FAE staff: service@adlinktech.com.